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Test Optimization of 2D SOC using Enhanced ACO Algorithm

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Abstract

With advancement in technology it is possible to design complex chips. To reduce the complexity of a chip, embedded cores based system-on-chip are being advocated. These complex chips require high test data volume which further increases the test application time. The cost of testing is dependent on total test application time. To reduce test application time, testing of cores should be done concurrently. This paper first proposes test solution using Ant Colony Optimization algorithm and then compares its performance using test time. Fork and merge technique is used for TAM sharing. Test time and TAM width of cores is selected using wrapper design algorithm. Experimental results on ITC'02 benchmark circuits for different widths of Test access mechanism (TAM) wires proves the effectiveness of one algorithm over the other.

Keywords: *SOC testing, power constraint, test bandwidth, ant colony optimization, greedy algorithm.*

1. Introduction

The rise in SOC complexity brings great challenges for testing. The modular approach proposed by Zorian et al. [1] for testing has been successful. In modular design, the design is partitioned into smaller blocks. Core based SOCs reuses predesigned and pre verified intellectual property (IP) cores to reduce the design cost and fasten the time to market process. In order to reduce the test time, testing of the cores should be done concurrently. There are some limitations like TAM sharing, power consumption during concurrent testing and hierarchical SOCs in which child cores are embedded inside parent cores. Therefore, test scheduling is considered as NP Hard problem and it can be represented as 2D bin packing problem[14]. Goel et. al. [15] proposed a method to calculate the test time in which each core has a wrapper and TAM optimization is done. Recently, papers on test scheduling with power constraint and hierarchical constraint are proposed [4][12][16]. Modular structure of a SOC is shown in Fig 1.

The basic components of modular approach for test optimization are:-

a).Wrapper Design – Some cores in a SOC have a dedicated wrapper design. The core inputs, outputs and scan chains are rearranged and linked to wrapper outside the core. The test vectors are applied to wrappers through TAM wires. Test time calculation of each core is done using wrapper design algorithm discussed in [2][3] and [4].

b).TAM optimization – Test vectors to be applied to SOCs are stored in ATE and are applied through Test access mechanism (TAM) wires. Different techniques like test bus [7][8][9] or fork and merge [18] can be used to transfer the test vectors from ATE to wrapper.

c).Test Scheduling –For testing, cores are scheduled such that we get the minimum test time. There are scheduling algorithms like RAIN[11], Particle Swarm optimization algorithm[10][12], Greedy algorithm[18] and genetic algorithm [13].There are various constraints that need to be considered during concurrent testing. Some of these are mentioned below:-

- Power constraint:- In case of concurrent testing, power consumption is needed to be considered as it can damage the chip[12].
- Hierarchical constraint:- In hierarchical SOCs, the parent cores should be tested along with the child cores.
- TAM width constraint:- In concurrent testing, the TAM width is limited. Therefore, TAM width constraint is needed to be considered for testing.
- TSV constraint:- In 3D SOCs, test data is transferred to different levels through silicon vias (TSVs). Recent Work on these SOCs is discussed in [19][20].

In this paper, we focus on how we deal with scheduling problem for SOCs. The main objective is to develop an efficient scheduling technique that can minimize the test time of the SOCs under the constraints of power, design hierarchy, TSV constraint and TAM width. Scheduling for SOC testing can be described using ACO algorithm[17].

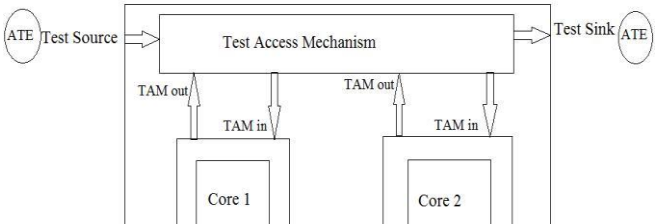

Fig 1:- Modular Structure of a SOC.

2. SOC Test Scheduling Problem Formulation

In this section, SOC test scheduling problem formulation is done. Let us consider a core based system with *n* no. of cores. Each core equipped with wrapper has TAM width to get access of test vectors. Each core has TAM width *tw*, power dissipation during testing *p*, test time calculated through wrapper design *tt*. The maximum allowed TAM width and power is *maxtw* and *maxp* respectively. *Remtw* and *Remp* is the remaining TAM width and remaining power during concurrent scheduling. The test time for each core can be calculated using wrapper design algorithm[2]. Test time can be calculated using the equation (1) :-

$$Test\ time = ((1+max(S_i , S_o)\ TP) + min\ (S_i ,S_o)) \quad (1)$$

S_i= input scan chain length.
S_o= output scan chain length.
TP= no of test patterns.

The total test time after scheduling for all cores can be calculated using the equation (2) :-

$$total\ test\ time = \min(\max \sum_{i=1}^{n} \sum_{j=1}^{maxtm} t_{ij}x_{ij}) \quad (2)$$

t_{ij} = test time for core i and tam width j.

x_{ij} = 0 or 1 which verifies that the core with that tam width is scheduled or not.

3. Enhanced ACO Based Test Scheduling Model

Ant colony optimization is based on real ant colony which is proposed in [17]. This is about the behavior of the ants, how they find the shortest path from their nest to the food. While searching for food, ants excrete a hormone called pheromone. Ants smell that pheromone and choose their ways that have high pheromone concentrations. During this process ants may find a shortest path due to pheromone trails left by ants from their nest to the food and back. The core selected for scheduling should follow these conditions:-

This paper is organized as follows. Section 2 discusses the SOC test scheduling problem formulation. Section 3 discusses the Enhanced ACO based test scheduling Model.. Section 4 presents the experimental results on ITC'02 benchmark circuits. Finally, Section 5 draws the conclusion.

$$tw <= remtw \quad (3)$$

$$p <= remp. \quad (4)$$

In enhanced ACO, the core selection for scheduling is done on the basis of *maxp* and *maxtw* and is partially dependent on probability as described by [17]. Firstly, a core is selected using probability, then it is tested using the constraints. If the conditions are satisfied, the core is selected. Otherwise, the core with next highest probability is tested. This step is repeated until all conditions are satisfied. Let us assume an ant *a* starts from a core *i* and has to reach out to other cores. The first core *i* is selected randomly and the next core *j* is selected using probability *prob*. This process is repeated until all cores are scheduled. Ant density model is used in this algorithm as described in [17]. According to Ant density model, the pheromone trail quantity left by ant through their paths is constant.

$$prob_{ij} = \frac{\tau_{ij}\eta_{ij}^{\beta}}{\sum_{i=0}^{n}\tau_{ij}\eta_{ij}^{\beta}} \quad (5)$$

$prob_{ij}$ = probability for core j as the next core to be scheduled.

τ_{ij} = pheromone trail value from path i to j >= 0;

η_j = It is the heuristic value which is dependent on the test time of the cores >= 0;

$$\eta_j = 1/tt. \quad (6)$$

β is a parameter used to enhance the heuristic value. Its value is higher for the hierarchical cores than the flat cores so that hierarchical cores can be tested first. When an ant moves from core *i* to *j* then pheromone trail needs to be updated through that path. This process is called trail intensification. The trail intensification can be formulated using equation (7):-

$$\tau_{(i\to j)} = \begin{cases} Q & if\ ant\ goes\ from\ i\ to\ j \\ 0 & otherwise \end{cases} \quad (7)$$

Enhanced ACO Algorithm

Input:

1. *n* = no of cores.
2. *maxtw* = maximum tam width available.
3. *maxp* = maximum power allowed.
4. core information:
   i. core number.
   ii. *tw* of the core.
   iii. *p* of the core.
   iv. *tt* of the core.
   v. *int u* to check whether the core is scheduled or not.

Output:

best_time = the minimized test time obtained after no of iterations.

begin

1. Initialize the pheromone matrix *τ[i,j]* and probability matrix *prob[i,j]*. *i* is the current core and *j* is the next core to be scheduled.
2. Before scheduling the value of *i* need to be initialized.
3. **For** all ants **do**
   Remtw=maxtw;
   Remp=maxp;
4. Exclude the pareto points of the core selected as i.
5. Update *remtw, remp, core end time,u* and *start_time;*
6. **For** 0 to *n*-1 **do**
7. Calculate the probability for core *j* and Update the *prob[i,j]*.
8. Select the core with maximum probability.
9. **if** tw_j <*remtw && p< remp* **then**
   Update *remtw,remp,u, core end time* and *start_time;*
10. **else**
11. Initialize an array which has *core end time* of all cores that are scheduled.
12. Sort the array in ascending order.
13. **For all** array values **do**
14. **if** tw_j<*remtw && p<remp* **then**
15. the core of this *core end time* is selected as start time.
16. *break;*
17. Update *remtw,remp,u,core end time* and *start_time;*
18. *τ[i,j]* is updated when a path is confirmed from *i* to *j*.
19. Value of *j* = Value of *i*
20. Test time is calculated after every core is scheduled.
21. Value of *i* is initialized for scheduling of next ant.
22. Calculate the best test time.

In this algorithm, the output is the minimum test time obtained after scheduling with several iterations.

4. Experimental Results

The proposed algorithm is applied to ITC'02 benchmark circuits like p93971, p22810 and d695. The test application time is calculated by varying the TAM size and maximum power limit p. The results of ACO algorithm for d695, p93791 and p22810 are compared with greedy algorithm in Table 1. Test time calculation with varying power dissipation is shown in Table 2, Table 3 and Table 4 for d695, p22810 and p93791 respectively.

Table1. Test time comparison of Enhanced ACO with previous work.

SOC	*Tam width (tw)*	*Greedy algorithm[18]*	*Enhanced ACO*	*[15]*
p22810	16	507 271	280 725	458 068
	32	271 377	190 511	222 471
	64	134 777	130 586	133 405
p93791	16	2 347 950	1 651 355	1 791 638
	32	1 008 396	877 738	912 233
	64	613 356	432 394	455 738

Table2. Test time with varying *maxp* for d695.

max tw	*maxp=1500*	*maxp=2000*	*maxp=2500*
16	57 869	55 777	55 777
32	31 947	25 791	25 791
64	21 755	17 540	14 605

Table3. Test time with varying *maxp* for p22810

maxtw	*maxp=6000*	*maxp=8000*	*maxp=10000*
16	280 775	280 775	280 775
32	290 511	290 511	190 511
64	176 663	173 292	130 586

Table4. Test time with varying *maxp* for p93791.

maxtw	*maxp=20000*	*maxp=25000*	*maxp=30000*
16	1 651 355	1 651 355	1 651 355
32	1 177 738	1 177 738	877 738
64	652 885	652 885	432 394

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