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Design of Low Power Wide Gates used in Register File and Tag Comparator

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Abstract

This paper presents a low power register file and tag comparator which has a lower leakage and higher noise immunity without affecting their speed due to wide fan in gates. Increasing leakage currents combined with reduced noise margins significantly degrade the robustness of wide dynamic circuits. Using low V_{th} 90 nm CMOS process technology model simulation of register files and tag comparators is designed. An improvement of 20% power reduction and 2 times noise immunity is observed in the implemented register file using the proposed circuit at the same delay compared to the standard domino circuits.

Keywords: *Low power, Leakage, Noise immunity, Wide fan-in, Domino logic*

1. Introduction

In many applications to achieve high performance, dynamic logic such as domino logic is widely used. Their performance is superior to that of static logic styles [1]. However, dynamic logic family suffers the drawback of susceptible to noise. On the other hand, due to technology scaling down, the supply voltage is reduced for low power, and the threshold voltage (V_{th}) is also scaled down to achieve better performances. But reducing the threshold voltage exponentially increases the subthreshold leakage current. Therefore, a reduction of leakage current and improved noise immunity are of major concern in robust and high performance designs in recent technology generations, especially for wide fan-in dynamic gates [2] which are typically employed in the read path of register files, L1 caches, match lines of TCAMs, flash memories, tag comparators, PLAs and wide MUX and De-MUX. The register files and tag comparators are more important in modern microprocessors since they are one of the most

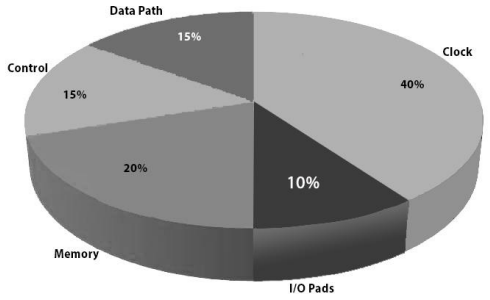

Fig. 1. Power dissipation in a typical CPU

critical modules in their critical paths [3]. To achieve remarkable performance by utilizing instruction level parallelism and memory locality, implementation of multi-ported register files and larger caches is necessary to feed data paths of multiple functional units and to store global variables for general-purpose microprocessors and embedded systems. Nevertheless increasing the switching capacitance due to the use of more transistors and larger on-chip components causes a significant increase in energy consumption. Therefore, the power dissipation of memory structures such as caches and register files will increase significantly with new generations of process technology.

2. Proposed Low power design

In dynamic logic gates leakage current of the evaluation network is substantially increased with technology down-scaling especially in wide domino gates, yielding lower noise immunity and higher power consumption.
So, to achieve desired noise robustness in wide fan-in gate, new design techniques are required. Besides, increasing the fan-in not only increases the worst case delay, it also increases the contention between keeper transistor and evaluation network.

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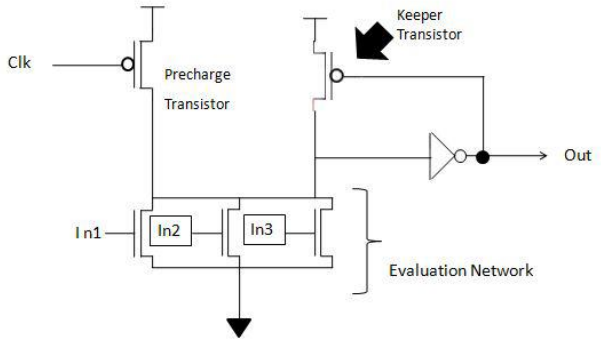

Fig. 2. Wide fan-in OR gates using the standard footless domino (SFLD).

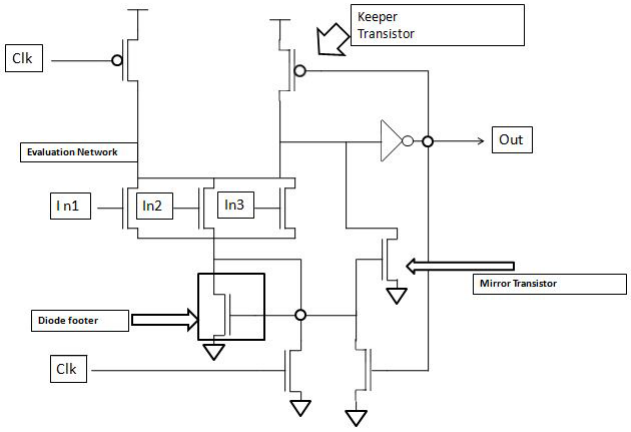

Fig. 3. Diode footer transistor configuration.

In the proposed circuit, a diode configuration transistor is added as a footer to provide more leakage current reduction when all inputs in the pull down network are at the low level or the circuit is set in the standby mode. This addition of diode-footer transistor results in a reduction of the subthreshold leakage of the evaluation network due to the stacking effect. The voltage drop due to the leakage current across this transistor decreases the subthreshold leakage in the following ways. First, it makes the gate to source voltage of the evaluation transistors negative. Second, it increases the body effect and consequently the threshold voltage of the evaluation transistors. Third, it decreases the drain to source voltage and DIBL of the evaluation transistors. Therefore, the leakage power of the circuit is decreased.

2.1 Design of register file

Execution cores of high performance microprocessors require multi-ported register file to execute independent instructions in parallel by multiple function units. In register files, Local (LBL) and global (GBL) bit lines of register files are typically implemented by wide dynamic circuits. However, the subthreshold leakage current of transistors increases exponentially with technology scaling, hence noise immunity of wide dynamic gates decreases rapidly. Although upsizing the keeper can improve circuit robustness, it increases delay and power consumption.

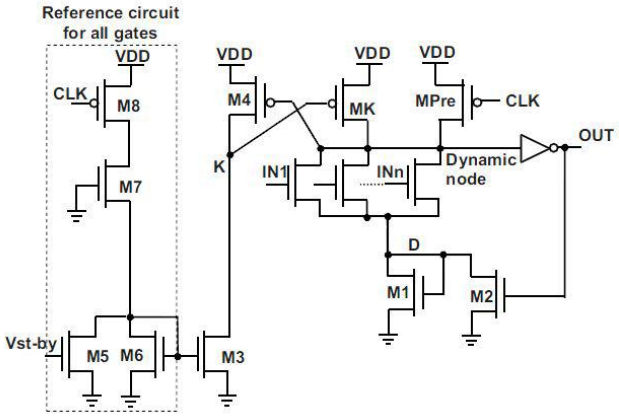

Fig. 4. The controlled keeper by current-comparison domino (CKCCD) [6]

As mentioned in [4], the bit line consumes a major portion of the dynamic power-nearly 70% in the register files and becomes the dominant factor in their energy breakdown. The power dissipation of the bit lines will be increased linearly by larger number of registers and higher number of ports.

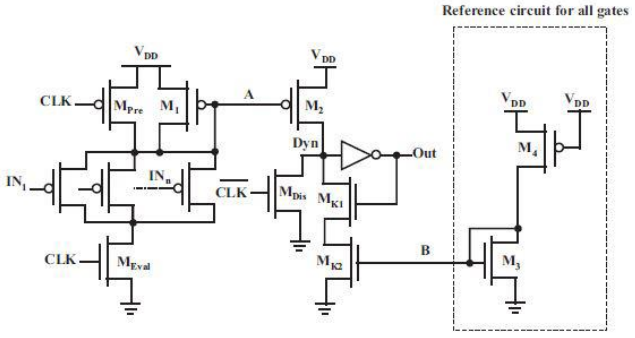

Fig. 5. The current comparison domino (CCD) for implementation of wide fan-in gates[7]

The leakage power consumption becomes a significant source of power consumption as the technology scales down even up to 50% in the 90nm technology [4]. Thus, reduction of bit line power consumption can reduce overall power consumption of register files and consequently total power of microprocessors.

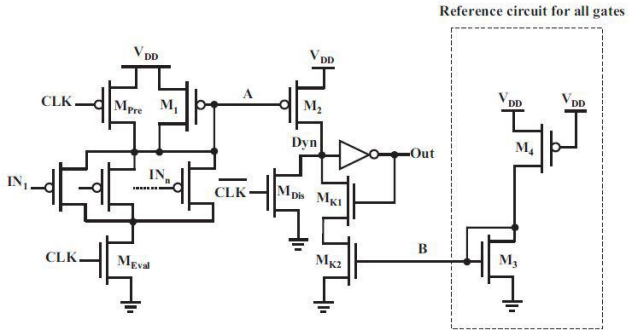

Fig. 6. The comparison-based dual-rail domino (CDL) [8].

To realize the local bit lines (LBL) with improved performance and robustness, we proposed several circuits such as CKCCD (Fig. 4) and CCD (Fig. 5). The use of this circuits allows us to use low threshold voltage to improve performance. These proposed circuits along with standard footless domino are implemented in a register file to demonstrate their ability for power reduction. The proposed register file is organized as follows.

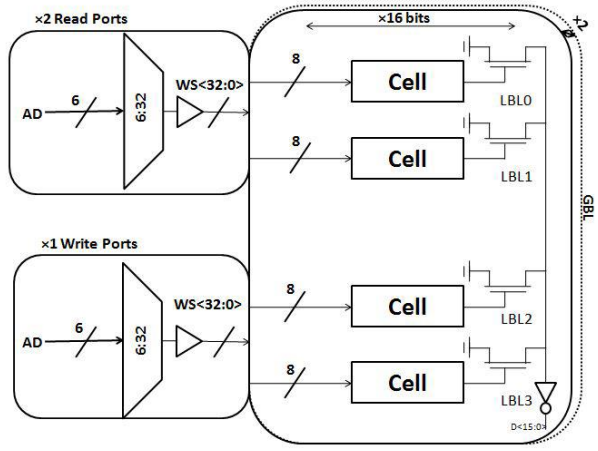

Fig. 7. 32-word × 16-bit register file organization.

As shown in Fig. 7, the organization of the 2-read, 1-write ported 32-word × 16- bit/word register file is used to compare several circuit techniques. A 6-bit read/write address per port is decoded using conventional static CMOS using two stages of 2 and 3-input NAND and NOR gates to provide the read/write select signals into the register file array. Chain of inverters with FO4 is used for driver and buffer circuits. As shown in Fig. 8, at the precharge phase of the clock cycle when CLK='0', $\overline{CLK}$ ='1' 32 D1 footed-domino buffers per port is used to drive the decoded read/write select signals and distribute across the 16-bit array width. Fig. 9 shows the register file bit cell, in which one read ports in each side of the storage cell is inserted to provide symmetric loading during cell write for optimal stability [5]. Demand for complement of the input data is removed by using an extra NMOS pass transistor. The full-swing local bit line (LBL) and global bit line (GBL) circuits implemented by the standard footless domino (SFLD) are shown in Fig. 10. (a) and (b). Each read port needs a LBL which forms a dynamic 16-way AND-OR. During read cycle, data from the storage cell is read by two transistors per word (M_1 and M_2) on each LBL. The GBL circuits, which are the same in all studied register files, are dynamic 8-input OR gates. These circuits deliver the 32-bit word per word read port from bit cells. In this paper LBL circuits of register files are implemented by the proposed circuits CKCCD and CCD to reduce power consumption as shown in Fig. 11. (a) and (b), respectively.

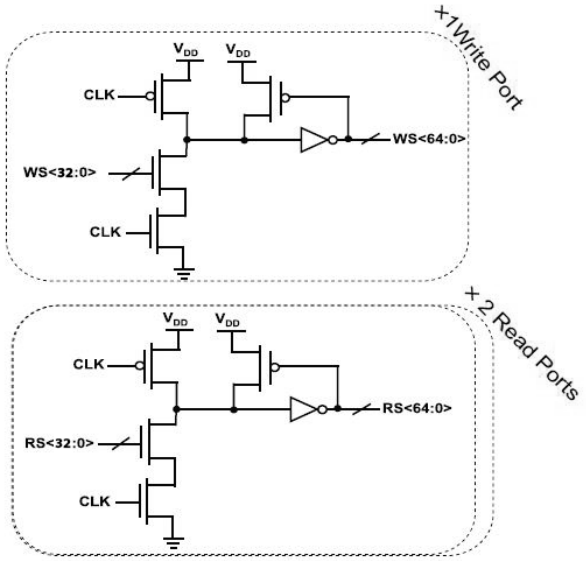

Fig 8. Read/write select D1 domino drivers.

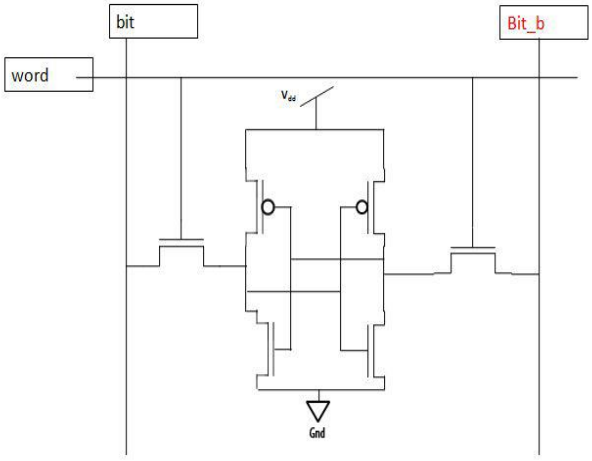

Fig. 9. 6T SRAM cell

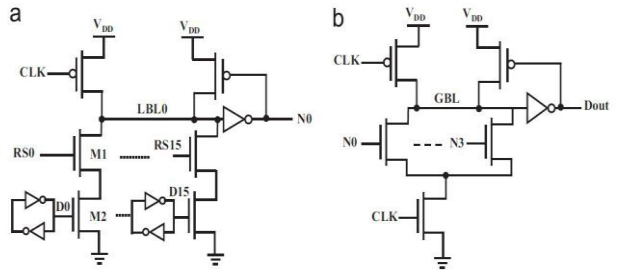

Fig. 10. (a) Local Bit line scheme. (b) Global bit line scheme.

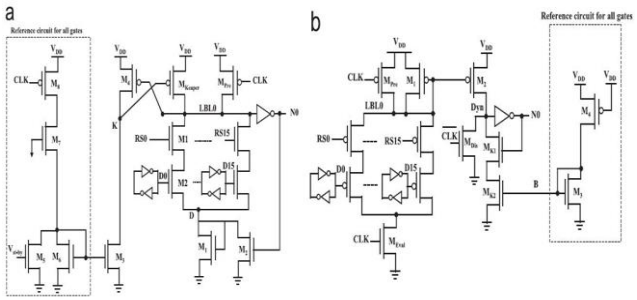

Fig. 11. Local bit line using the proposed circuit (a) CKCCD (b) CCD

2.2 Design of Tag comparator

Another module which plays an vital role in compensating the low speed of off-chip main memory against high speed processor is cache. Thus, a power efficient microprocessor needs larger on-die cache memories with higher hit rate to boost their speed. One of the major critical paths in modern microprocessor, a cache memory generally consists of a tag comparator, a tag SRAM and data SRAM. Although many research have been done to design high-performance cache, the processor-memory performance gap is still growing due to several reasons. One of them is tag comparator, since until its hit/miss signal is not ready for the cache controller; cache cannot continue to complete its function.

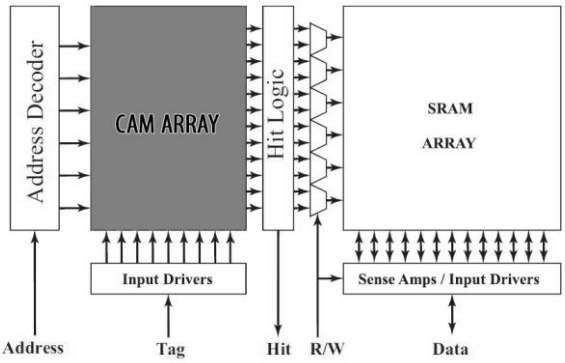

Fig. 12. Highly associative CAM-tag cache organization

Conventional tag comparator designs are widely implemented by wide fan-in domino circuits. As physical address space and number of tag bits are increased in every generation, delay and power consumption of tag comparators which employ these high fan-in domino circuits are strongly increased especially in deep sub-micron (DSM) technologies with higher subthreshold leakage.

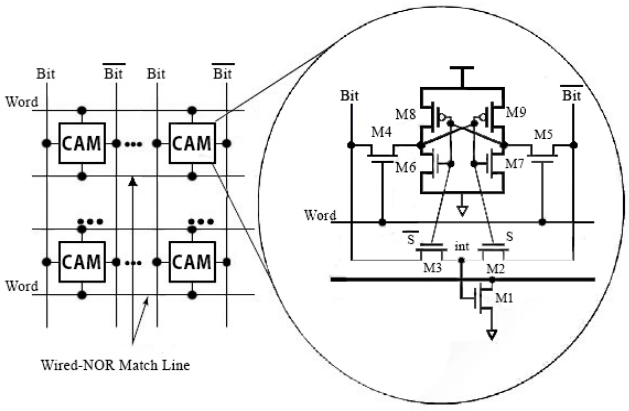

Fig. 13. CAM cell using 9 transistors.

The power consumption of the cache due to the tag comparators increases when high-way set-associative caches or content addressable memory (CAM) tags are used to increase hit rate. Organization of a highly-associative CAM-tag cache and CAM cell circuitries are shown in Figs 12 and 13, respectively.

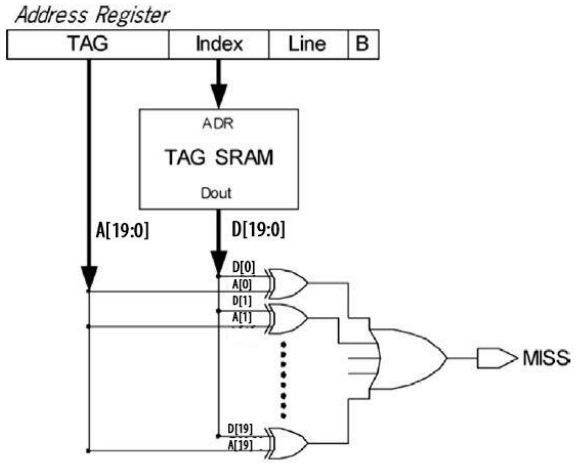

Fig. 14. Tag SRAM and tag comparator.

In this paper, a standard 10-transistor is used for CAM cell which is composed of a SRAM cell and a dynamic XOR gate employed for comparison, as shown in Fig. 14.
The match line is connected to all CAM cells in a row and initially precharged to V_{DD} and conditionally discharged on a mismatch. All match lines must be connected as wired-OR to generate the hit/miss signal.

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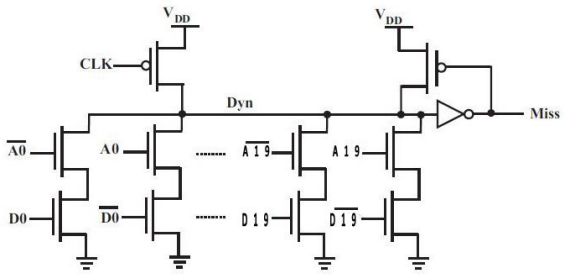

Fig. 15. The 20-bit tag comparator implemented by standard footless domino(SFLD).

A 20-bit tag comparator which is required for 32-bit microprocessors with 25-bit physical address, is implemented using a 2-input XOR and a 20-bit OR gate, as shown in Fig. 14 [9]. The 20-bit input tag address is compared with 20-input data from the tag SRAM or CAM by the tag comparators. Since speed is critical, all tag comparisons are done in parallel at the expense of extra power consumption. If a match line is found a cache-line replacement occurs.

In this paper, tag comparators are implemented using single-rail version of our proposed circuit technique called CDL (Fig. 6) to reduce delay and power consumption of

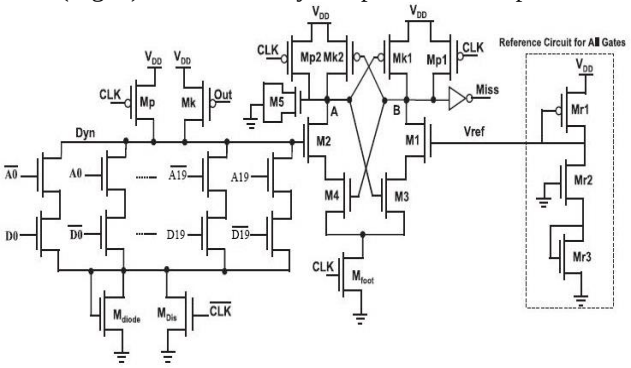

Fig. 16. The 20-bit tag comparator implemented by single version of the comparison-based dual-rail domino (CDL).

the wide fan-in tag comparators and high switching capacitance during a search operation. In order to reduce the energy dissipated on the tag comparators due to heavy switching capacitance, the voltage swing on the match lines or the dynamic node, Dyn in Fig. 16. M_5 is used as a MOS capacitor to equalize load capacitance on the nodes A and B as shown in figure. Lowering the power consumption of the tag comparators helps us employ CAM-tag caches for embedded systems and gain benefits of their higher hit rate which results in lower access energy due to the lower misses.

3. Simulation results

3.1 Simulation were done using TANNER software, version 14.0.

Circuit models	Parameter	
	Power (µw)	Delay (ps)
SFLD	178	19.62
LCR	168	17.38
CKCCD	143	19.37
CCD	133.38	23.88
CDL	121.73	25.23

3.2 Register file simulation

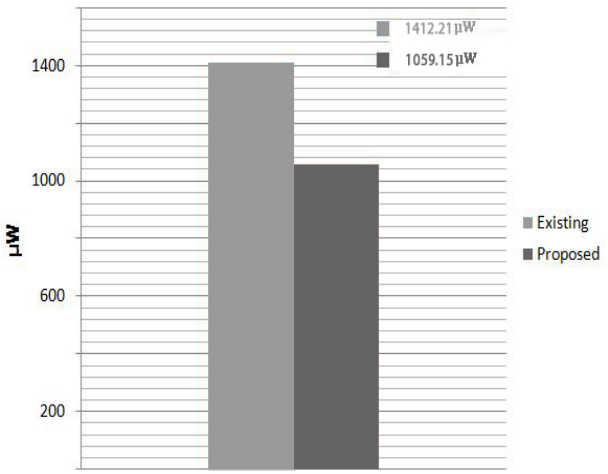

Fig. 17. Comparison of existing and proposed model in terms of power dissipation.

3.3 Tag comparator simulation

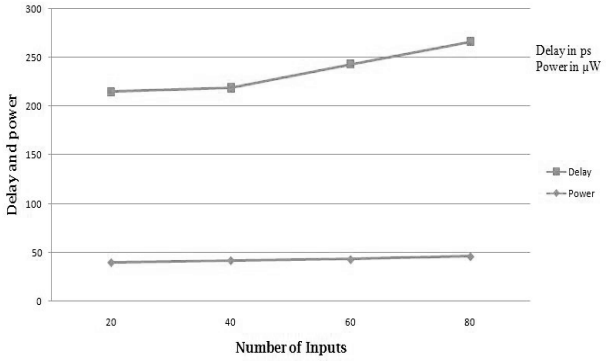

Fig. 18. Relationship between delay and power consumption of the tag comparator used CDL circuits in terms of the number of input.

4. Conclusions

Wide dynamic gates are used to implement read path of register file and tag comparators of caches. Register files are critical units in data path and are frequently used in processors. Cache memories are also located between data path and main memory to enhance performance. Register files and caches are the dominant components of the total power consumption in the embedded processors mainly due to their frequent use. In modern superscalar processors, the read and write ports of the register files increase to support parallel operations of several functional units to enhance process speed. Therefore, power efficient processors can be obtained by reducing the power consumption of the caches and the register files. Since the implemented register file using CKCCD technique and the tag comparators designed by CDL technique presented approximately 20% and 15% respectively lower power consumption compared to the standard footless designs in the same noise immunity, the proposed circuits CKCCD and CDL used in the register files and CAM caches, can reduce total amount of the power consumption in embedded processors significantly.

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