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FPGA Implementation of State Machine Controller of Transmitter for Wi-Fi

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Abstract

The paper presents the implementation of State Machine Controller of Transmitter for Wi-Fi. Design method uses very-high-speed integrated circuit hardware description language (VHDL). The code is then implemented on Virtex-II Platform FPGA i.e. device- xc2v250, package-fg456 and speed grade -4. This device belongs to the Virtex–E group of FPGAs from Xilinx. Simulations verify the functionality of the designed transmitter. The transmitter design matches well with the theoretical expectation of IEEE 802.11. With a maximum frequency of 128.791MHz, minimum run-time for the simulation took 7.765ns.

Keywords –IEEE 802.11, Wi-Fi, VHDL, Transmitter, FPGA

I. Introduction

Wireless communication is a fast growing technology that enables people to access networks and services without cables. IEEE 802.11(Wi-Fi) is a communication protocol standard that defines a physical layer and a MAC layer for wireless communication within a short range (from a few meters up to 100 m) with low power consumption (from less than 1mw up to 100 mw). Wi-Fi is oriented towards computer-to-computer connection as an extension of or substitution for cabled LANs [1].

The Wi-Fi MAC is an adaptation of the wired Ethernet MAC, and therefore uses carrier-sense before transmission (also known as "listen before talk"). Unlike wired Ethernet, the Wi-Fi MAC cannot detect collision. So, Wi-Fi dictates that every received packet is acknowledged by an "acknowledgement" (ACK). If a station or access point transmits a packet and does not receive an ACK from its target recipient, it assumes that a collision with another Wi-Fi transmission has occurred. To avoid additional Wi-Fi collisions, the station uses an exponential back-off algorithm (i.e., pauses a few micro-seconds) and transmits again [2].

Like wired Ethernet, Wi-Fi supports true multipoint networking with such data types as broadcast, multicast, and unicast packets. Although standard practice is approximately one access point (AP) to every 10-20 stations (STA), the MAC address built into every device allows for a virtually unlimited number of devices to be active in a given network. These devices contend for access to the airwaves using a scheme called Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). The Wi-Fi physical layer uses direct-sequence spread spectrum (DSSS) at four different data rates using various modulation techniques to communicate. The transmit power level can vary, but is typically between 30 and 100 mW (+15 to 20 dBm) [2].

The widespread availability of 802.11-based hardware has made it the premier choice of both researchers and practitioners for developing new wireless networks and applications. However, the ever increasing set of demands posed by these applications is stretching the 802.11 MAC protocol beyond its intended capabilities. For example, 802.11 provide no control over allocation of resources, and the default allocation policy is ill-suited for heterogeneous environments and multi-hop networks [3].

The wireless MAC has been designed in many papers with 802.11a specification. There are several implementation methods, such as CPU-Based, Cell-Based and FPGA. With CPU-Based, it has advantage of flexible design, but complex, low process speed and will cost high. With Cell-based, it has advantage of simple design, high process speed and easy for simulation, but design is non-flexible and need long developing time. FPGA has both of advantages of CPU-based and Cell-based, such as high process speed, flexible design and short developing time [4].

Here, Wi-Fi MAC transmitter module(Fig 1) is divided in to 5 blocks i.e. Data Unit Interface block, State machine controller block , Pay Load Data Storage block , MAC Header Register block , Data Processing block. FPGA implementation of Pay load data storage block and Data

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processing block is already presented [5].Similarly, FPGA implementation of MAC header block was also presented [6]. In this paper, we are considering only one block i.e. State machine controller block. So, other blocks are not discussed further in this paper.

II. MAC Frame format

To meet the challenges posed by a wireless data link, the MAC was forced to adopt several unique features. All stations shall be able to properly construct frames for transmission and decode frames upon reception. Each frame consists of the following basic components [4],

a. MAC header: Contains frame control, duration ID, address (1~4) and sequence control information;

b. Frame body: Contains information specific to the frame type in variable length (0~2312 bytes).

c. Frame check sequence (FCS): IEEE 32 bit Cyclic Redundancy Check (CRC). It contains result of applying CRC-32 polynomial to MAC header and frame body.

A General frame format

The MAC frame format comprises of a set of fields that occur in a fixed order in all frames. Figure 1 shows the generic 802.11 MAC frame, field are transmitted from left to right.

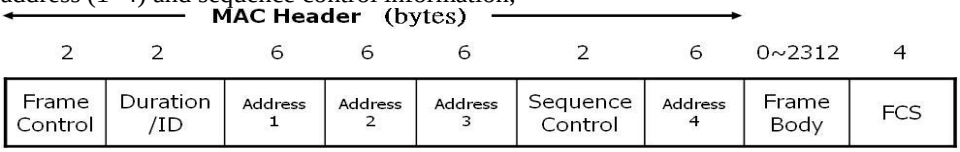

Figure 1 Generic 802.11 MAC frame

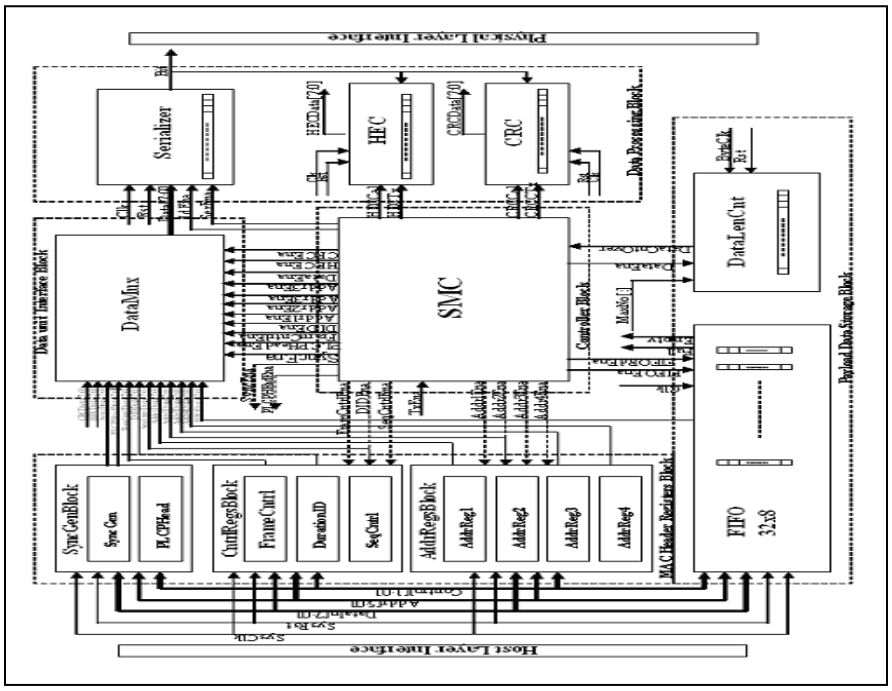

Fig 1 Wi-Fi MAC Transmitter Module

III. State Machine Controller

A. State machine in VHDL

Only one state machine per module is considered and is expected to be completely synchronous. Any structural logic like multiplexers, counters, etc are not included in the state machine. All the flip-flops are to be clocked at the same clock. Having multiple clocks will complicate the design and optimization to a greater extent. So, dedicated clock and reset are used. To implement a state machine in VHDL, the state diagram is the only requirement. In VHDL, each state of state machine is translated in to a case in a "case-when" construct and is simply one of the case statement branches. State transitions are specified using "if-then-else" statements [7].

B.State Diagram

The frame give in the section 2 is 802.11 frames and the main idea is to how to generate it. First, we are in idle state until RST=0, when TXEna signal received from the upper layer. The 1st thing is to generate preamble bit so next state

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is preamble bits so next state comes is Sync SFD, we stay there up to 80-bit sequence of alternative '0' and '1' and SFD bits, then sync over goes '1' and the next state will be PLCD, it passes its PLCP Header and make PLCP Header Over '1' and move to HEC which is pass HEC code and make HEC Over '1' and then moves to Frame Control State. At this state, required frame control bit is sent and making frame control over '1'. After the transmission of the frame control bits, it moves to DID state which provide suitable ID and make DID Over '1', and move to ADDER1 state.

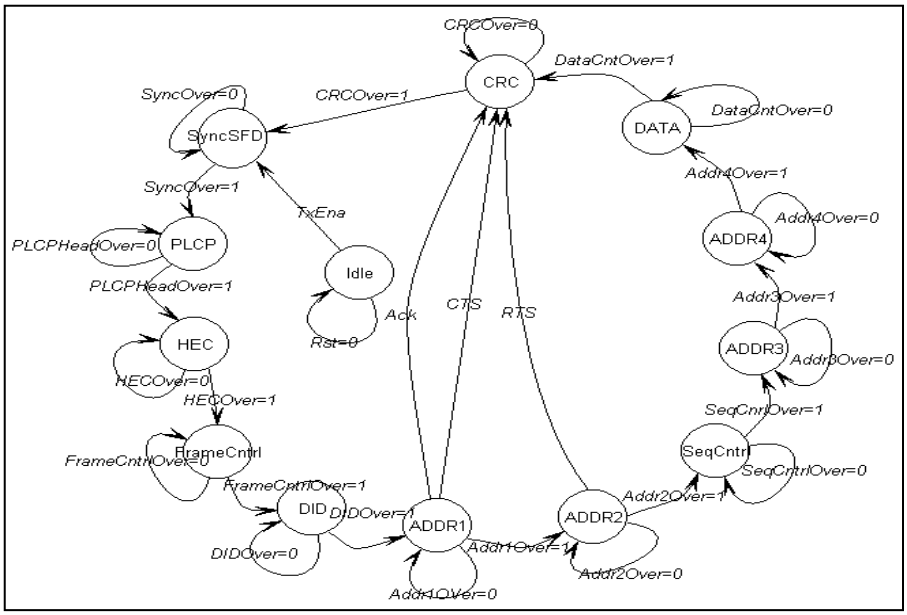

Fig 2 State Diagram of the Wi-Fi Transmitter

In Wi-Fi transmission before any data is sent a small request frame is sent i.e. a RTS. This RTS is generated by flowing from state Idle to state ADDRE2 followed by CRC. Now in similar way CTS & ACK is generated.

After RTS or CTS frame we have to send the data which is having the frame format given by the Fig.4.5. So the next state followed is the SeqCntrl, which provides the sequence control information. When the SeqCntrl Over signal becomes '1' then ADDER3 & ADDER4 states are followed simultaneously to give the required address. Now after providing the address, the DATA state will come and the whole data is transmitted and DataCnt Over goes to '1'. Then comes the CRC state to send the CRC bit and goes to again SyncSFD state when the CRC Over becomes '1'.

C. State Machine Controller:

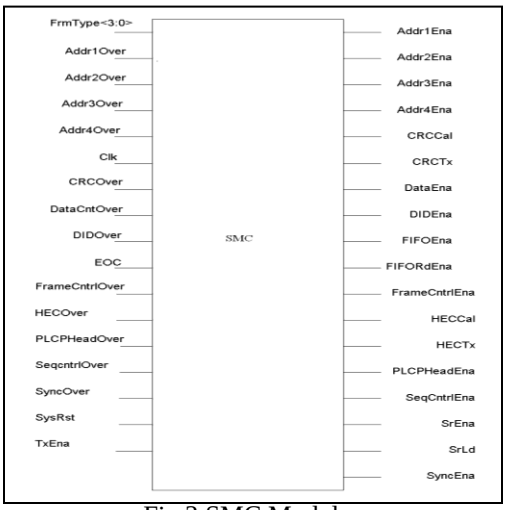

Fig 3 SMC Module

Description: It is the heart of the entire circuitry. It controls the working of all modules sequentially. Simulation wave form of SMC is shown in Fig 4.

Simulation Results:

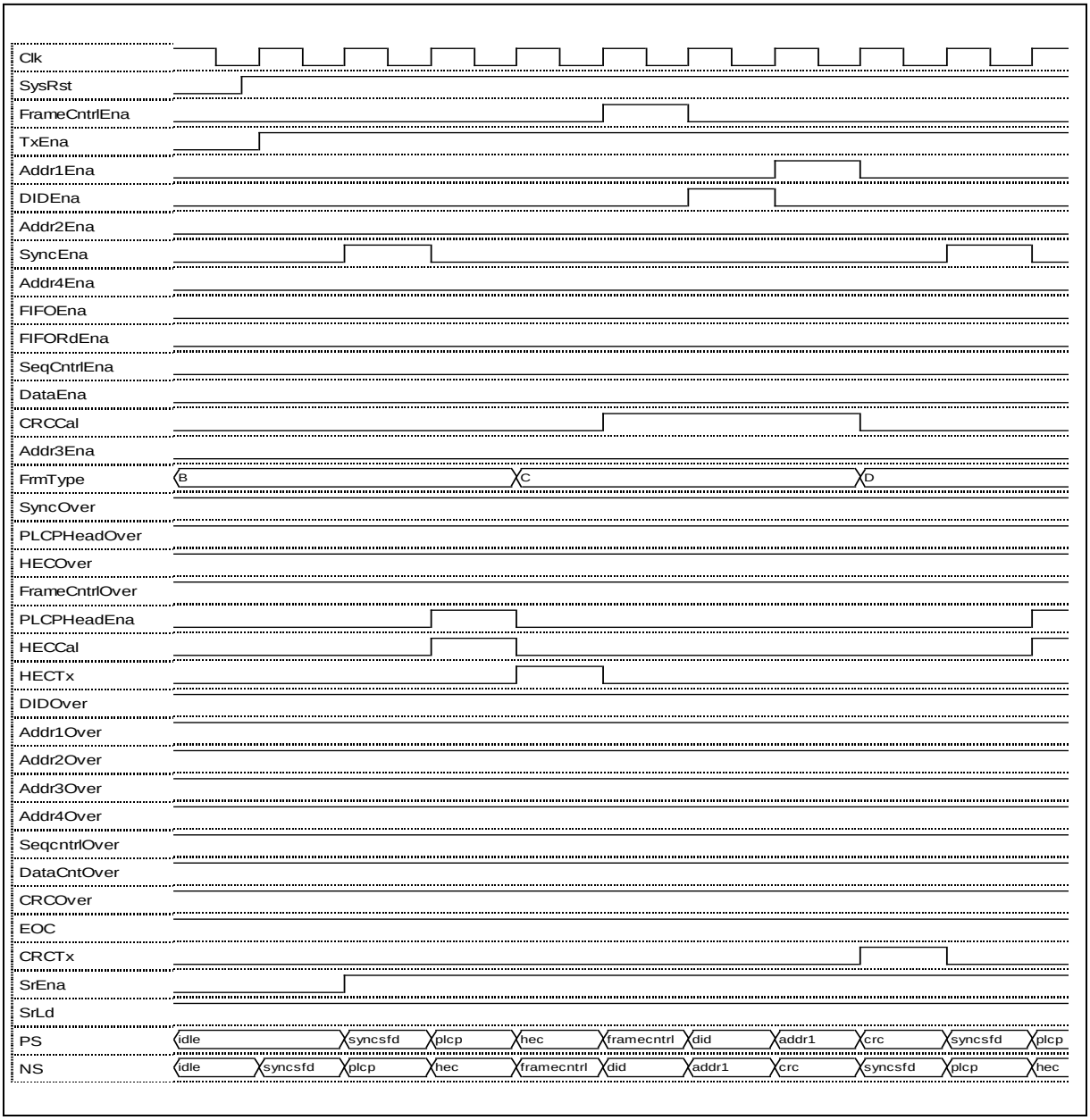

Fig 4 Waveform of SMC Module

D. Top Module: Top module is shown in Fig 5.The simulation of the top module is divided in to 5 different parts and the simulated waveforms are shown in Fig 6, Fig 7, Fig 8, Fig 9 and Fig 10.

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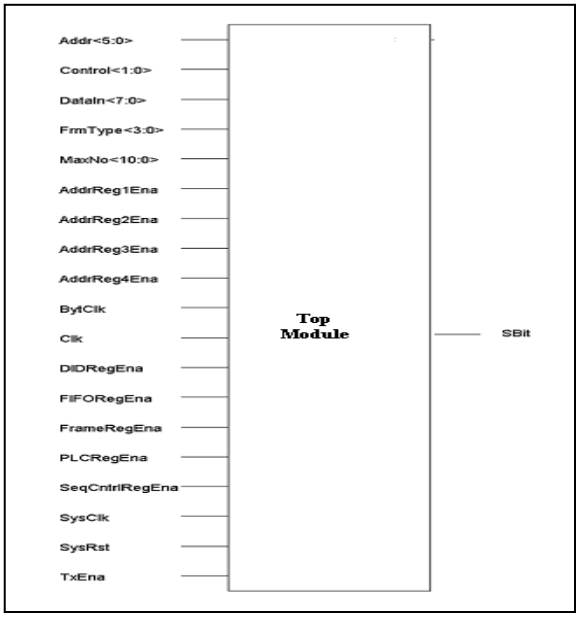

Fig 5 Top Module

Simulation Results: First Part

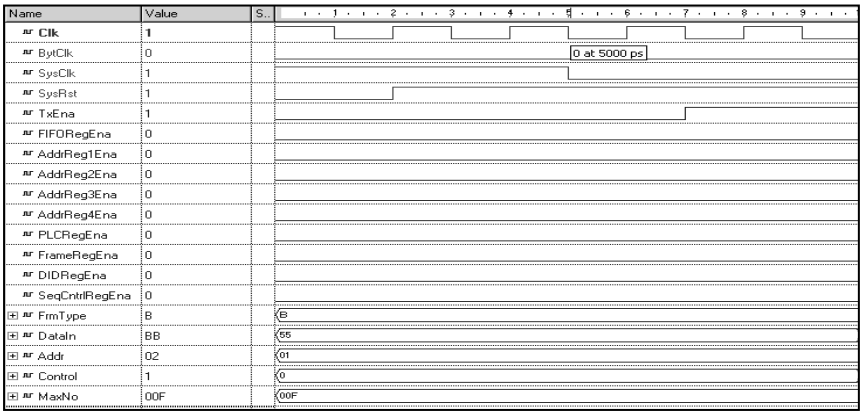

Fig 6 Waveform of Top Module (First part) Second Part:

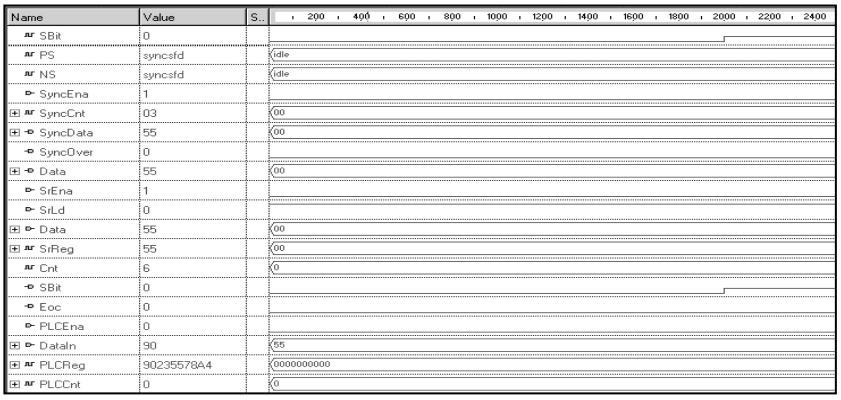

Fig 7 Waveform of Top Module (Second part)

Third Part:

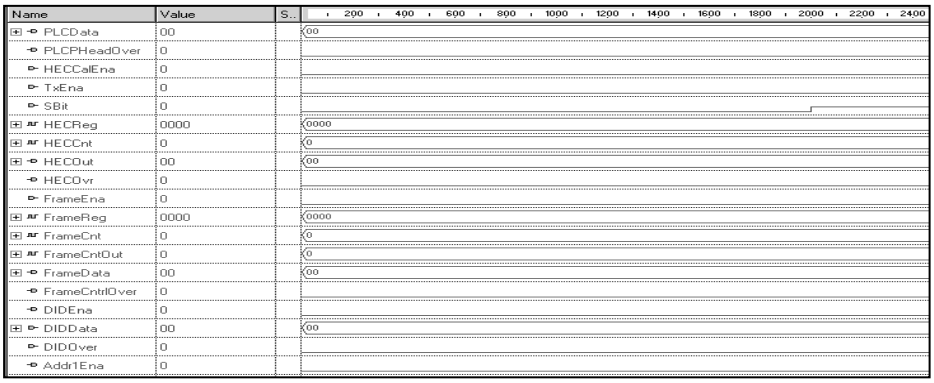

Fig 8 Waveform of Top Module (Third part)

Fourth Part:

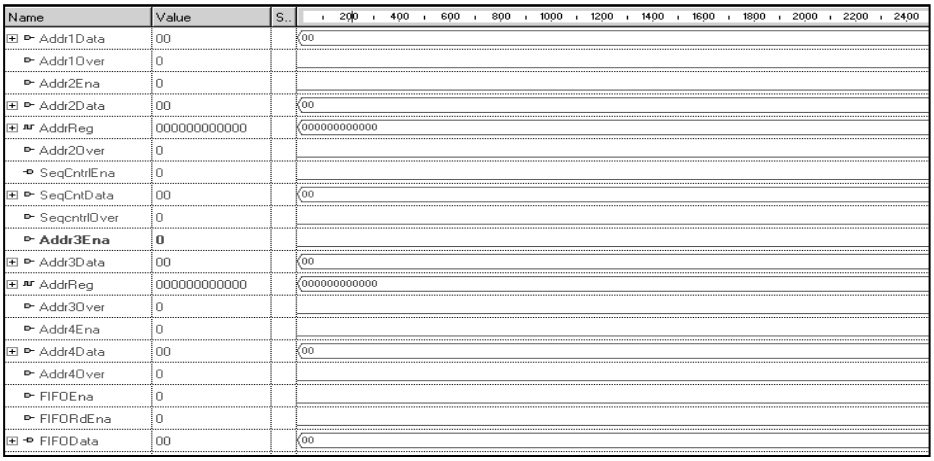

Fig 9 Waveform of Top Module (Fourth part)

Fifth Part:

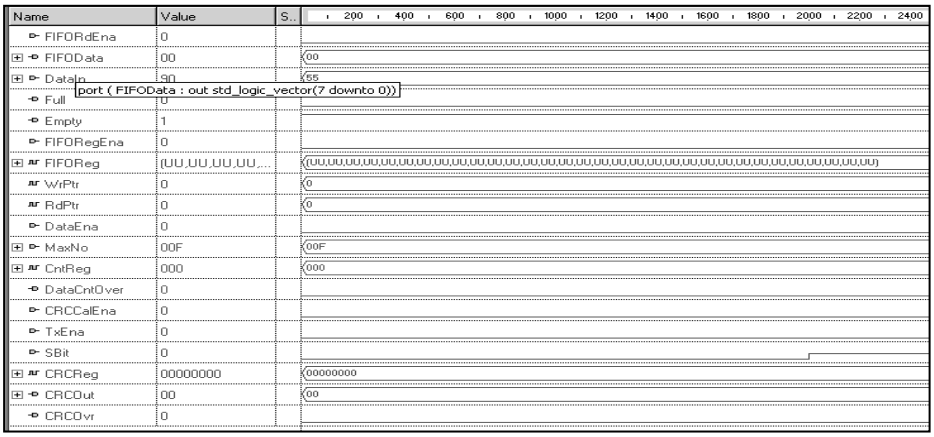

Fig 10 Waveform of Top Module (Fifth part)

IV. Conclusions

Various individual modules of Wi-Fi Transmitter have been designed, verified functionally using VHDL-simulator, synthesized by the synthesis tool, and a final net list has been created. This design of the Wi-Fi Transmitter is capable of transmitting the frame formats. The formats include all 802.11 frames viz MAC Frame, RTS Frame, CTS Frame and ACK Frame. This transmitter is also capable of generating error-checking codes like HEC and CRC. It can handle variable data transfers, i.e. 0-2312 bytes of data can be transmitted. A brief summary of the synthesis is presented at the end of this paper.

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Brief Summary of Synthesis

Target Parameters

Output File Name	: top-model
Target Device	: XC2V250-4FG456

Device utilization summary:

Selected Device: XC2V250-4FG456

Number of Slices:	720 out of 1536 46%
Number of Slice Flip Flops:	926 out of 3072 30%
Number of 4 input LUTs:	982 out of 3072 31%
Number of bonded IOBs:	39 out of 200 19%
Number of GCLKs:	3 out of 16 18%

Timing Summary:

Speed Grade: -4

Minimum period	: 7.765ns (Maximum Frequency: 128.791MHz)
Minimum input arrival time before clock	: 7.768ns
Maximum output required time after clock	: 5.446ns
Maximum combinational path delay	: No path found

Timing Detail: All values displayed in nanoseconds (ns)

Timing constraint	: Default period analysis for Clock 'SysClk'
Delay	: 6.538ns (Levels of Logic = 33)
Source	: M8_WrPtr_1 (FF)
Destination	: M8_WrPtr_31 (FF)
Source Clock	: SysClk rising
Destination Clock	: SysClk rising
Data Path	: M8_WrPtr_1 to M8_WrPtr_31
Gate Net Cell	: in->out fanout Delay Delay Logical Name (Net Name)

Total 6.538ns (4.925ns logic, 1.613ns route)

(75.3% logic, 24.7% route) Total memory usage is 96568 kilobytes