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A Low Power High Speed Adders using MTCMOS Technique

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Abstract

Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. Two important attributes of all digital circuits, for most applications are maximizing speed and minimizing power consumption. The speed of different modules used in the design will dominate the overall performance of the system. Depending on the delay and power consumption requirements, several adders can be implemented in many ways such as carry look-ahead (CLA), carry-skip adder (CSA) and ripple carry adder (RCA). The main objective of this paper is to provide new low power solution for Very Large Scale Integration (VLSI) designers. MTCMOS is an effective circuit-level technique that provides a high performance and low-power design by utilizing both low and high-threshold voltage transistors. MTCMOS technique has been proposed in this paper and the proposed technique has small power dissipation as compared to CMOS technique. Simulations based on BSIM 3V3 180nm CMOS technology.

It shows 4 bit adders of the proposed technique have low power dissipation as compared CMOS technique.

Keywords- RCA, CLA, CSA, power, MTCMOS technique.

1. INTRODUCTION

In recent years, the growing demand for high-speed arithmetic units in floating point co-processors, image processing units and DSP chips has led to the development of high-speed adders as addition is an obligatory and indispensable function in these units. Computations in these devices need to be performed using low-power, area-efficient circuits operating at greater speed. Depending on the area, delay and power consumption requirements, several adder implementations, such as ripple carry, carry-skip and carry look-ahead are available in the literature.

Digital integrated circuits commonly use CMOS circuits as building blocks. The continuing decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. Excessive power dissipation in integrated circuits, not only discourages their use in portable environment but also causes overheating, reduces chip life and degrades performance. Minimizing power dissipation is therefore important, both for increasing levels of integration and to improve reliability, feasibility and cost [1]. Power dissipation can be reduced by scaling the supply voltage. The scaling of supply voltage linearly with feature size was started from half-micron technology. But the power supply scaling affects the speed of the circuit .The need of the time is to put efforts in designing low-power and high speed circuits. MTCMOS technology has emerged as a promising alternative to build logic gates operating at a high speed with relatively small power dissipation as compared to traditional CMOS. MTCMOS is an effective circuit-level technique that provides a high performance and low-power design by utilizing both low and high-threshold voltage transistors [2]. This technology is used for reducing subthreshold currents in standby mode while maintaining circuit performance.

2. ADDERS

2.1 One Bit Full Adder

A one-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs a, b and c_{in} and two outputs S and C_{out} [3] as illustrated in Fig. 1.Expressions for S and C_{out} are given in (1) and (2)

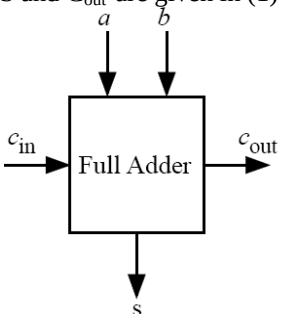

Figure 1.A full adder block

$$S = a \oplus b \oplus c_{in} \quad (1)$$

$$C_{out}=a.b+b.c_{in}+c_{in}.a \quad (2)$$

2.2 Four Bit Ripple Carry Adder

A simple ripple carry adder (RCA) is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain. Fig. 2 shows the

interconnection of four full adder (FA) circuits to provide a four bit ripple carry adder.

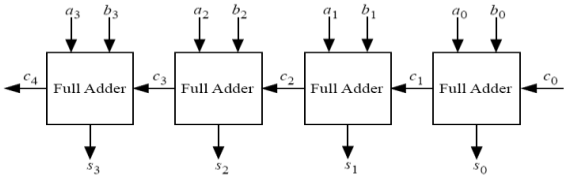

Figure 2.Four bit ripple carry adder

Notice from Fig. 2 that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits a_0 and b_0 in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits $S_0 - S_3$. The main problem with this type of adder is the delays needed to produce the carry out signal and the most significant bit [4]. These delays increase with the increase in the number of bits to be added.

2.3 Four Bit Carry Look Ahead Adder

The carry look-ahead adder (CLA) solves the carry delay problem by calculating the carry signals in advance, based on the input signals. It is based on the fact that a carry signal will be generated in two cases: (1) when both bits a and b are 1, or (2) when one of the two bits is 1 and the carry-in is 1. Thus, one can write [5]

$$c_{i+1} = a_i . b_i + (a_i \oplus b_i). c_i \quad (3)$$

$$S_i = (a_i \oplus b_i) \oplus c_i \quad (4)$$

The above two equations can be written in terms of two new signals P_i and G_i, which are shown in Fig. 3.

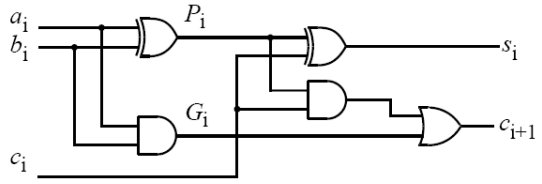

Figure 3.Full adder at stage *i* with *Pi* and *Gi* shown

$$c_{i+1} = G_i + P_i . c_i \quad (5)$$

$$S_i = P_i \oplus c_i \quad (6)$$

Where,

$$G_i = a_i . b_i \quad (7)$$

$$P_i = a_i \oplus b_i \quad (8)$$

G_i and P_i are called the carry generate and carry propagate terms, respectively. Notice that the generate and propagate terms only depend on the input bits and thus will be valid after one and two gate delay, respectively. If one uses the above expression to calculate the carry signals, one does not need to wait for the carry to ripple through all the previous stages to find its proper value. Let's apply this to a four bit adder to make it clear. Putting i=0,1,2,3 in (5) we get [5]

$$c_1 = G_0 + P_0 . c_0 \quad (9)$$

$$c_2 = G_1 + P_1 . G_0 + P_1 . P_0 . c_0 \quad (10)$$

$$c_3 = G_2 + P_2 . G_1 + P_2 . P_1 . G_0 + P_2 . P_1 . P_0 . c_0 \quad (11)$$

$$c_4 = G_3 + P_3 . G_2 + P_3 . P_2 . G_1 + P_3 . P_2 P_1 . G_0 + P_3 . P_2 . P_1 . P_0 . c_0$$

(12)

Fig. 4 shows that a four bit CLA is built using gates to generate the Pi and Gi signals and a logic block to generate the carry out signals according to (9)–(12).The disadvantage of CLA is that the carry logic block gets very complicated for more than four bits. For that reason, CLAs are usually implemented as four bit modules and are used in a hierarchical structure to realize adders that have multiples of four bits.

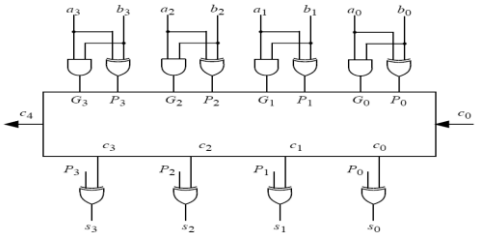

Figure 4. Four bit Carry Look Ahead Adder implementation

2.4 Four Bit Carry Skip Adder

A carry skip adder (CSA) is designed to speed up a wider adder by adding the propagation of a carry bit around a portion of the entire adder. A carry skip logic is illustrated in Fig. 5 for the case of a four bit adder. The carry in bit is C_i and the adder itself generates carry our bit of C_{i+4}.

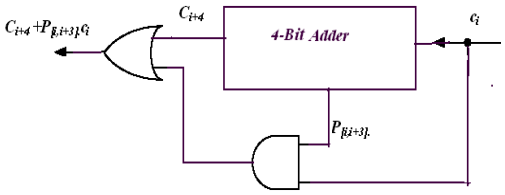

Figure 5.Carry skip logic

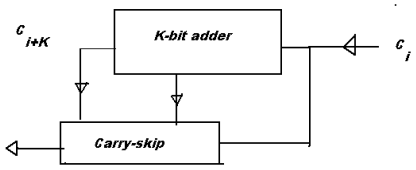

Figure 6.Generalization

The carry skip circuitry consists of two logic gates [5]. The AND gate accepts the carry in bit and compares it to the group propagate signal using the individual propagate values. The AND gate output is give

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$$P_{[i,i+3]} = P_{i+3} . P_{i+2} . P_{i+1} . P_i \quad (13)$$

ORed with C_{i+4} to produce a stage output of

$$Carry = C_{i+4} + P_{[i,i+3]}.c_i \quad (14)$$

As shown in the Fig. 5 if $P_{[i,i+3]} = 0$ then the carry out of the group is determined by the value of C_{i+4}. However, if $P_{[i,i+3]}=1$ and the carry-in bit is $C_i=1$,the group carry-in is automatically sent to the next group of adders. The name carry skip is due to the fact that if the condition $P_{[i,i+3]}.c_i$ is true, then the carry in bit skips the block entirely. Fig. 6 shows generalization to a *k* bit adder.

3. CMOS TECHNIQUE

In CMOS (Complementary metal oxide semiconductor configuration) design the circuit topology is complementary push pull in the sense that we have both PMOS and NMOS networks in the circuit. Consequently, both the devices contribute equally to the circuit operation characteristics. There are three major sources of power dissipation in digital CMOS circuits which are summarized in the following [6]

$$P_{avg} = P_{switching} + P_{short\text{-}circuit} + P_{leakage} = \alpha_{0->1} C_L \cdot V_{dd}^2 \cdot f_{clk} + I_{sc} \cdot V_{dd} + I_{leakage} \cdot V_{dd} \quad (15)$$

The first term represents the switching component of power, where C_L is the load capacitance,f_{clk} is the clock frequency and $\alpha_{0->1}$ is the probability that a power consuming transition occurs (the activity factor).The second term is due to the direct-path short circuit current, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations [7],[8].

4. MTCMOS Technique

Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the subthreshold leakage current [9]. In modern high performance integrated circuits (ICs), more than 40% of the total active mode energy can be dissipated due to the leakage currents. With more transistors integrated on-die, leakage currents will soon dominate the total energy consumption of high performance ICs. A popular low leakage circuit technique is the Multithreshold Voltage CMOS (MTCMOS).

The multi threshold CMOS technology has two main features. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip [10]. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as "power gating". The schematic of power gating technique using MTCMOS is shown in Fig. 7.The transistors having low threshold voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate

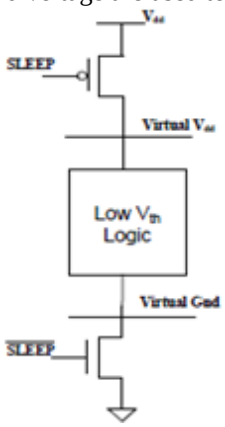

Figure 7.Power Gating Technique using MTCMOS.

the low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation [11].

In the active mode, sleep transistors are turned on and the logic consisting of low V_T transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high V_T transistors are turned off causing isolation of low V_T transistor from supply voltage and ground thereby reducing sub-threshold leakage current.

5. COMPARISON AND RESULT

Implementation of 4 bit RCA,CLA and CSA using CMOS, MTCMOS technique have been done at 180 nm BSIM3V3 technology. Power dissipation comparisons of 4 bit RCA,CLA and CSA using CMOS and MTCMOS technique over supply voltage (V_{dd}) range are shown in Fig. 8 to Fig. 10.Simulation results for power dissipation are shown in Table I. Fig. 8 shows power dissipation comparison graph for four bit RCA using CMOS and MTCMOS technique for different values of supply voltages (V_{dd}). Here Fig. 8 depicted that MTCMOS RCA reduces 53.58% power dissipation than CMOS RCA at supply voltage of 1.0V.

Fig. 9 shows power dissipation comparison graph for four bit CLA using CMOS and MTCMOS technique for different values of supply voltages(V_{dd}) .Here Fig. 9 depicted that MTCMOS CLA reduces 54.75% power dissipation than CMOS CLA at supply voltage of 1.4V.

Fig. 10 shows power dissipation and power delay product comparison graph for four bit CSA using CMOS and

MTCMOS technique for different values of supply voltage(V_{dd}) .

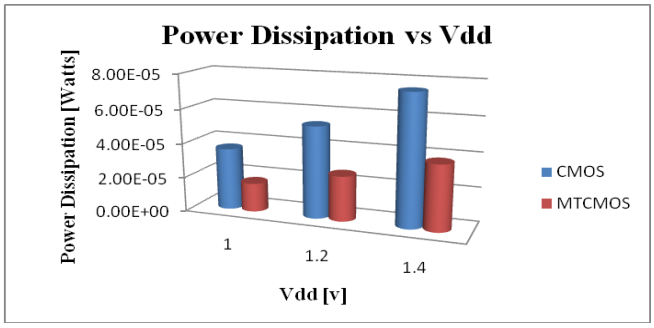

Figure 8.Power dissipation comparison of four bit RCA using CMOS and MTCMOS technology.

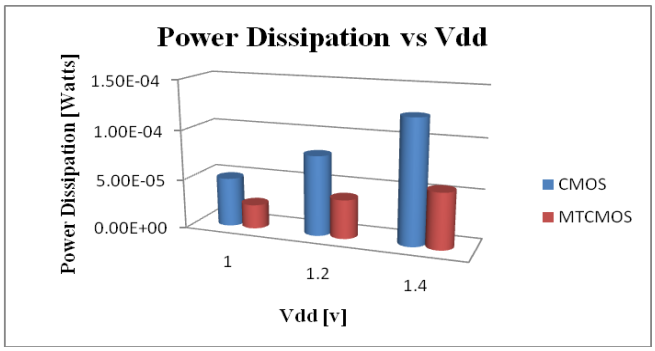

Figure 9.Power dissipation comparison of four bit CLA using CMOS and MTCMOS technology.

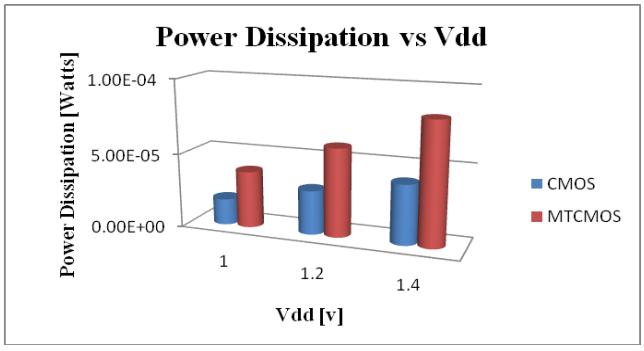

Figure 10.Power dissipation comparison of four bit RCA using CMOS and MTCMOS technology.

Here Fig. 10 depicted that MTCMOS CSA reduces 53.65% power dissipation than CMOS CSA at supply voltage of 1.0V.After comparison we can conclude
that MTCMOS technique based adders have least power dissipation.

6. CONCLUSION

A four-bit RCA, CLA and CSA circuits based on MTCMOS technique have been proposed. The analysis of the simulated results confirms the feasibility of the MTCMOS technique in RCA, CLA and CSA and shows that there is reduction of 50 to 53 percent in the value of power dissipation parameter as compared CMOS technique at supply voltage of 1V. MTCMOS adders have a marginal increase in area compared to the CMOS adders; overall, we achieved the lowest power dissipation.

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TABLE I. SIMULATION RESULTS OF RCA, CLA AND CSA FOR POWER DISSIPATION OVER VARIOUS SUPPLY VOLTAGES

Adders Type	Power Dissipation(10^{-5})					
	VDD =1.0V		*VDD=1.2V*		*VDD=1.4*	
	CMOS	***MTCMOS***	***CMOS***	***MTCMOS***	***CMOS***	***MTCMOS***
RCA	3.598	1.67	5.32	2.61	7.52	3.785
CLA	4.93	2.43	8.04	3.91	12.4	5.61
CSA	3.84	1.78	5.95	2.97	8.22	4.01

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