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Router RTL Design for Network on Chip (NoC) with Common Resource Sharing Scenario by Arbitration Technique

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Abstract

Now a day's System of Chip (SoC) is becoming more complex one due to the integration of more than hundred IP cores on a single chip. There is introducing a concept of Network on Chip in silicon industries to decouple communication and computation. The router is the backbone of Network on Chip (NoC).

The main goal of this research work is to focus on efficient router design with Verilog Hardware Description Language (HDL).We have designed, analyzed and verified top-level architecture for a router with submodules FIFO, FSM, Register, Synchronizer, and Arbiter. Xilinx 14.5 IDE with Spartan-3E- xc3s100e FPGA family has been used for the design of router. We analyzed power consumption with XPower analyzer and memory utilization with post-synthesis report. Research work proves that with acceptance of few delays, efficient router design can be possible which reduces thrice of the area as well twice of power consumption and that is the need of silicon industry.

Keywords*: Network on Chip (NoC), Router, FIFO, FSM, Synchronizer, Arbiter.*

1. Introduction

IC designers have innumerable challenges to design a single IC with thousands of circuits including billion of transistors over it. System on Chip (SoC) comprises of a number of IP cores on a single chip. There is introducing the concept of NoC in SoC, to decouple communication from the computation in IP cores.

Network topology plays an important role while deciding a number of routers per IP core. There is a number of topologies in which IP cores can connect with each other like mesh, tree, and hybrid topology. For example, mesh topology with 3x3 ports will require 3 numbers of routers to work design properly, this concept has already discussed in many research work. But in present work we focus on NoC design where few delays of response are acceptable in communication means the connection between IP cores having different speed. We have implemented dynamic priority arbiter for getting grant over the single router to allow multiport communication. Router designed with a top-level architecture having FSM, FIFO, Synchronizer and Register as submodules. In present work, we customized router input-output protocol to allow multiple input ports try to communicate with a number of output ports for serial communication based on adaptive priority.

The remainder of this paper starts by discussing Background and evolutions of NoC described in Section-2.concept of Network on Chip under section-3. Section-4 contains a description of fundamental support by the router in NoC. Section-5 contains our proposed architecture for router design. Section-6 contains the simulation and coverage reports. We conclude this paper with Section-7 with highlighting the efficiency of router design over existing one.

2. Network on Chip-Related Work

In 2004, NoC design is proposed as a future of ASIC design [1].In 2008, Survey on NoC carried out and published as a whitepaper [2]. In 2012, the importance of Network on Chip to decouple communication from computation with its advantages described and efficient router design with CDMA approach analyzed [2, 3]. In 2014, Five port router designed for NoC with single resource sharing concept, FSM controller and held as a special issue in an international conference in ICCSP [4].In 2015, a Top level architecture for router designed and index-based round robin arbiter designed for the router in [5,6].In 2016, there is more focus on router input and output protocols as well as the performance of the router design [7,8]. There is one whitepaper published by Arteris IP, This whitepaper summarizes the limitations of traditional bus-based approaches, introduces the advantages of the generic concept of NoC, and provides

specific data about Arteris NoC, the first commercial implementation of such architectures [9]. New concepts and techniques are emerging as a research to get more efficient router design for NoC.

3. Network on Chip-Concept

Network on a chip contains three building blocks Links, Router, Network Interfaces. Links provide an actual physical connection between different IP cores. Routers are intelligent blocks that provide set of rules and policies in the transmission mechanism. Network interfaces provide logical connections between IP cores

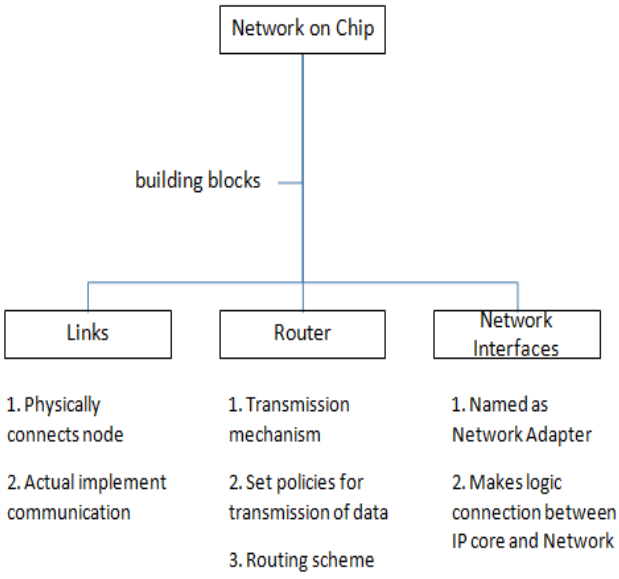

Fig.1 Basic building blocks of NoC[2].

4. Fundamental support by Router

The router in NoC decides set of rules and policies for transmission of data from one port to other. Design of router provides five fundamental supports. 1st Header and payload calculations to avoid misplace of data, the router decides the first byte of a packet as a header from which it internally calculates the length of the payload. Synchronization is to ensure correct transfer of data. Buffer empty and full condition checking is to avoid loss of data. Parity checking is to ensure faithful transmission of data. The internal soft facility is to detect corrupted data by checking response time.

Data transmission in the router is carried out in the form of packets. Hence router supports packet switching based synchronous protocol. The packet is having the first byte as a header of width 8-bit. A number of payloads each of 8-bit and length of the payload is internally calculated from first 6 MSB bits of header while LSB 2-bits of a header used for address identification. The last byte of the packet is known as Parity which ensures faithful transmission of data.

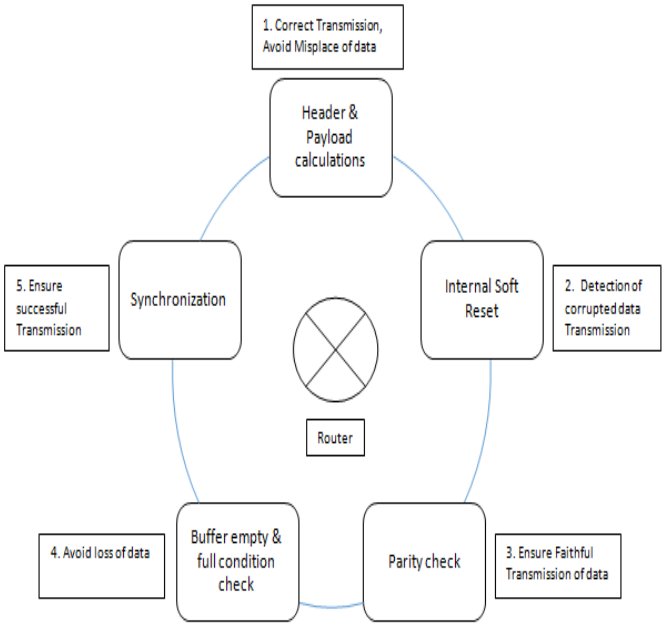

Fig.2 Fundamental Support by Router in NoC[5].

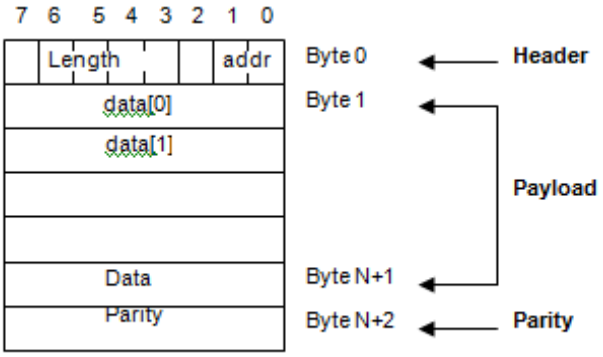

Fig.3 Packet Format[7].

5. Proposed design

In present work, we focus on common resource sharing. A scenario where a group of IP cores contains some IP's having fast computation speed and some having comparatively low speed. By perceiving today's challenge of area and memory in chip design, this concept of common resource sharing scenario has been proposed here. Tree topology for connection of IP nodes considered. Router 1x3 designed having an only single input port and three output ports. Whenever 3 source IP nodes try to communicate with 3 IP nodes (client node), grant assigned to that one who is having current highest priority. The source node having highest priority can only share router and take part in communication.

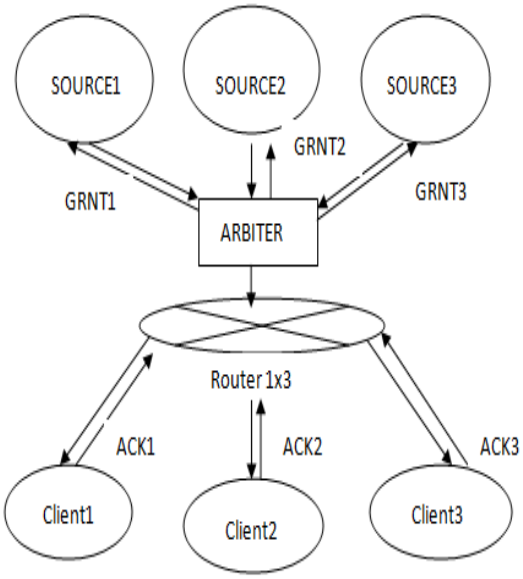

Fig.4 Common Resource sharing

Arbiter for the same has been designed with dynamic adaptive priority scheduling type. In which there is an internal counter which gives timeout signal. Whenever access to router denied and another router getting highest priority depends on the request queue. This type of Arbiter eliminates the problem of starvation and due to automatic update of priority, all source nodes get chance to share a router.

5.1 Top Level Architecture

Router designed using FSM controller, Synchronizer, Register, FIFO as submodules.
Top level architecture designed with integration of Arbiter and router.

Arbiter Module has req_0, req_1, req_2 as input signals from source nodes and gnt_0, gnt_1, gnt_2 as output signals. When a source node wants to send data to the router it must send a request to the arbiter. Assignment of the grant to source node is decided by arbiter FSM and source having grant can only send Data. In the Idle state, req_0 has given highest priority then req_1 and last req_2. Example, when req_0 asserted by source_0 with data_in1 then grant_0 assigned to source_0 and at the same time counter starts to give a specific time to send data to the router. If at the same time if req_1 and req_2 asserted then it will check timeout and assign grant by checking buffer.
Here buffer is an internal register which stores the status of availability of data with node. If arbiter assign grant to the node and there is no data available with that node it will update the value of buffer. Accordingly that status of the buffer it will switch priority among three source nodes.

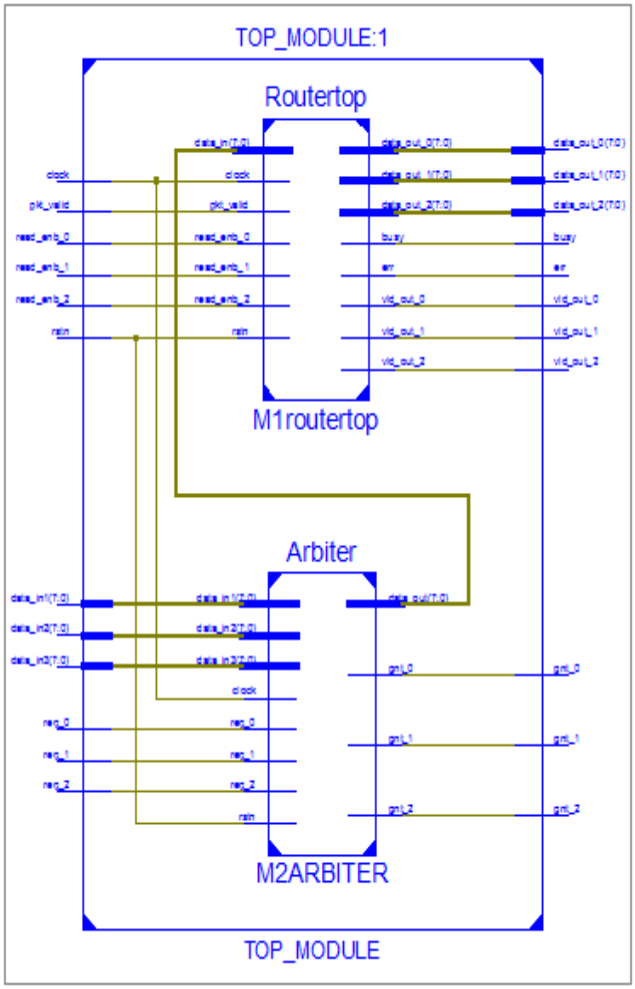

Fig.5 Top Level Architecture

After synthesis of dynamic arbiter, RTL obtained

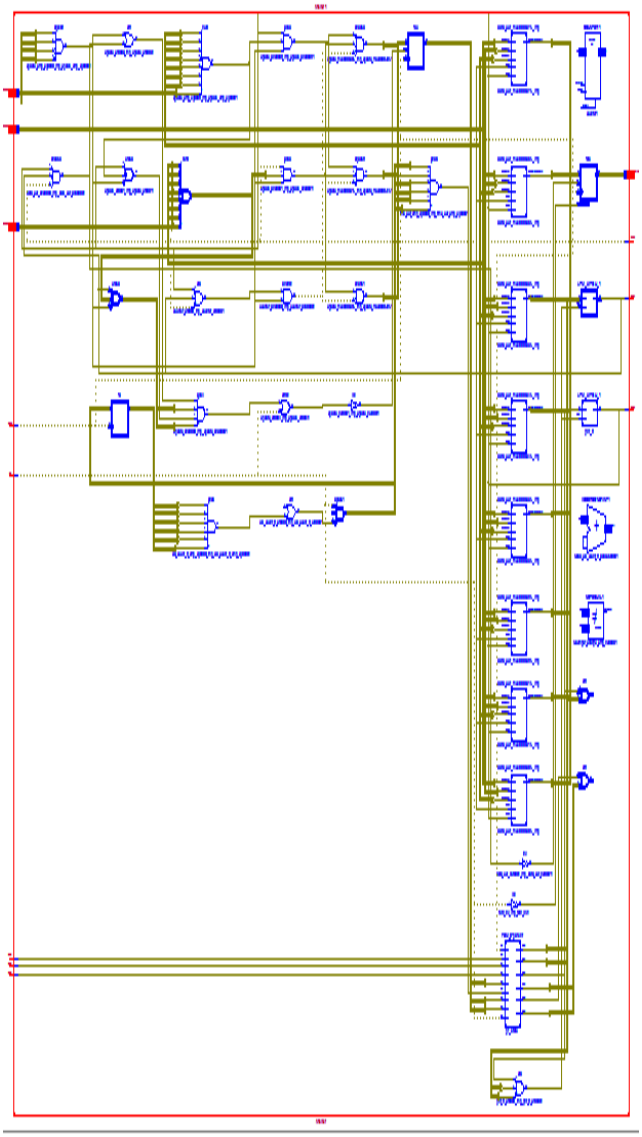

Fig.6 RTL view of Arbiter

5.2 Router1x3 Architecture

Router 1x3 designed with sub-modules like FSM, Synchronizer, Register and FIFO out of which FSM is signal generator type controller that monitors as well as send control signals to each sub-block of the router. There are three FIFO, one for each destination node. FIFO is storing element with 16x8 byte size. Whenever there is no data with FIFO, it generates an empty signal indicating the availability of free space in the buffer and when it found that data is going to overwrite then it generates a full signal.

Synchronizer module checks the validity of received data, it checks the status of buffer and if found to be empty then generates data validity signal. Synchronizer provides internal soft reset facility.

Register module has parity checking facility, it contains logic for internal parity calculations and by comparing that internal parity with external one it asserts error signal. Error signal indicates corrupted data.

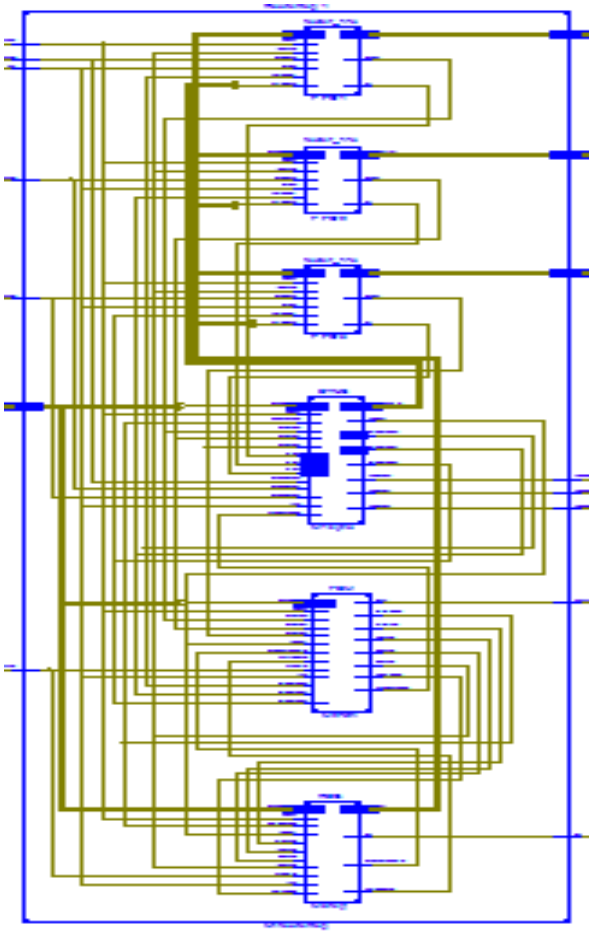

Fig.7 Router1x3 Architecture

6. Simulation and Coverage reports

ISim simulator of Xilinx 14.5 used to verify the design. Layered test bench used for verification of the design. Code coverage of design observed on Questasim. From the simulation of design, it is observed that design is working as per input-output protocol of router.

Layered test bench provides advanced verification environment. Different test cases used to verify proper working of router design such as FIFO full scenario, parity miss match scenario, soft reset condition check, actual

payload transmission. From all that cases we come to know that router with arbiter is working properly.

Arbiter with dynamic priority observed on ISim

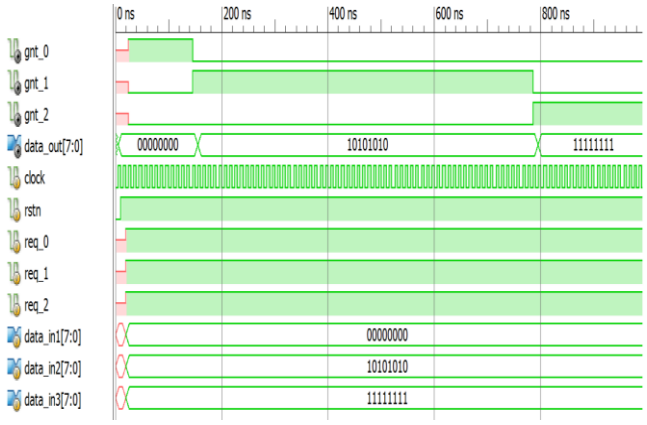

Fig.8 Arbiter waveform

Complete design of router with arbiter simulated on ISim and waveforms observed. There are 3 data inputs and 3data output ports. On every positive edge data observed on output port with the accurate transmission as per router policies

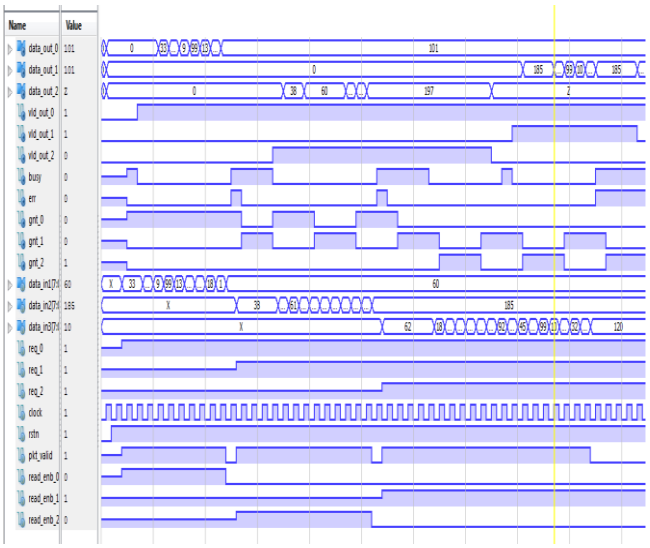

Fig.9 Router with Arbiter waveform

We have calculated code coverage for the Top module and observed it is 81.43% almost all FSM states have been visited only there is some toggle type missed.

Code coverage obtained by Questasim. The router is synchronous protocol and accepts data on positive edge clock with the active low reset signal. With Spartan-3E xc3s100e FPGA family we are getting frequency 100MHz. on Spartan-6 xc6slx4 FPGA device family we are getting 172.32 MHz. Here we have the result of the area and memory utilization with Spartan -3E FPGA family. 277.22 MB memory required for design on Spartan -3E FPGA family while power consumption analyzed on XPower analyzer and found 33.59 mW. While single resource sharing of the router with the same architecture of router1x3, it takes the memory of 831.66 MB and power of 80mW with Spartan-3E FPGA family. We have device utilization report as Table 1 and code coverage report as Table 2.

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	334	1,920	17%	
Number used as Flip Flops	310			
Number used as Latches	24			
Number of 4 input LUTs	481	1,920	25%	
Number of occupied Slices	376	960	39%	
Number of Slices containing only related logic	376	376	100%	
Number of Slices containing unrelated logic	0	376	0%	
Total Number of 4 input LUTs	489	1,920	25%	
Number used as logic	481			
Number used as a route-thru	8			
Number of bonded IOBs	65	66	98%	
IOB Latches	4			
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.99			

Table 1: Device Utilization

Coverage Summary by Structure:		Coverage Summary by Type:				
		Weighted Average:				81.43%
Design Scope	**Coverage (%)**	**Coverage Type**	**Bins**	**Hits**	**Misses**	**Coverage (%)**
TOP_MODULE_tb	81.43%	Statement	324	297	27	91.66%
dut	79.61%	Branch	146	126	20	86.30%
		FEC Expression	6	6	0	100.00%
		FEC Condition	98	68	30	69.38%
		Toggle	612	340	272	55.55%
		FSM State	8	8	0	100.00%
		FSM Transition	21	15	6	71.42%

Table 2: Code coverage of Top Module

Conclusions

A common resource sharing scenario for different speed of IP cores proposed in this paper. The proposed design has been verified with Verilog HDL on Xilinx 14.5 IDE. Simulation clearly states about router protocol. Device utilization observed on Spartan 3E FPGA family. Post-synthesis report and XPower analyzer reports observed for proposed design and from that here we conclude, Router design with Arbiter technique saves up to thrice of the area and twice of power in common resource sharing scenario. The only delay of few ns added due to the common router but if in case of acceptance of little delay we can say that proposed system of the router in NoC can be an efficient one.

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Biography

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