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Effect of Gate Work-function on Gate Induced Drain Leakage of MOSFETs

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Abstract
The impact of Gate induced drain leakage (GIDL) on the overall leakage of sub-micrometer 90nm N-channel metal–oxide–semiconductor field-effect transistor (NMOS) is modeled & simulated using SILVACO TCAD Tool. The drain current characteristics has been plotted & analyzed using ATLAS which shows how drain current varies with gate voltage at constant drain voltage. Value of GIDL current is estimated from these characteristics and compared with analytical model of GIDL. LDD and work-function engineering is used to improve leakage current of the device. This work gives a systematic study & simulation of the Gate Induced Drain Leakage current reduction by changing the gate work-function. The leakage current of the MOSFET decreases, as the work-function of the poly-silicon gate increases from 4.0~5.2 eV,

Keywords: *GIDL, LDD, MOSFET, BTBT*

1. Introduction

Over the past 50 years of the semiconductor industry, the size of metal–oxide–semiconductor field-effect transistor (MOSFET) has been scaled down obeying the Moore's law: feature sizes of transistors are scaled at a rate of approximately 0.7 times every 18 months. In the past few decades, the major concerns of the VLSI designers were performance and miniaturization but as the device size in decreasing day by day, the major focus are on reducing leakage currents. In the last few years we have substantial growth in portable computing and wireless communication and in this area, power dissipation has become a critical issue. As device is scaled down, problems with heat removal and cooling become worse because the magnitude of power dissipated per unit area is increased [1].
The reasons behind the leakage currents are explained in the following few lines. First reason is that as we scale down device, sub-threshold conduction increases exponentially with the threshold voltage reduction. Threshold voltage is reduced because all voltages applied to the device are also scaled with device dimensions.

Second one is that the surface band-to-band tunneling (BTBT) increases exponentially due to the reduced gate oxide thickness. Gate oxide thickness is also reduced in scaling device dimensions. Third reason is that the bulk BTBT increases exponentially due to the increased doping concentrations in bulk and well. The GIDL current occurs due to the conditions present in the immediate gate-to-drain overlap region. This current is very sensitive to the oxide geometry under the edge of the gate. The maximum value of the electric field in drain region is increased by an imperfect optimization of the drain structure and the gate to drain overlap.

2. Gate Induced Drain Current

GIDL is a band to band tunneling phenomenon and an off-state leakage current mechanism. GIDL current is a result of depletion at drain surface below the gate drain overlap region. When the drain is connected to a positive bias and the gate is in the vicinity of zero bias or to a negative bias, the n+ drain region under the gate is depleted and even inverted under the influence of vertical electric field acting in the x direction. Due to the accumulated holes at the surface, the surface behaves like a p-region which is more heavily doped than the substrate. The depletion region formed near the drain is formed narrower due to heavy doping in the drain region. When the gate is at large negative bias and drain is at large positive bias then the drain region (drain gate overlap region) will be depleted and even inverted. The high electric field causes band bending between gate and drain. Physically, BTBT is characterized by electron tunneling across the silicon band-gap from the inverted drain surface into the quasi-neutral drain. These electrons travel towards the drain as GIDL current. Valence e-and holes, left behind by the tunneling process, are then free to transport into the body region of the device under the influence of the lateral electric field giving rise to substrate related reliability issues and thus completing the path for GIDL current. Under very high electric field conditions, the generated hot gets trapped in the oxide leading to oxide breakdown [2]. The high energy electrons may easily pass through the gate oxide resulting in gate leakages. Also as the effective channel length decreases, the ratio of gate to drain overlap to whole device size becomes larger and as result of this maximum lateral electric field moves from channel to gate drain

overlap region because LDD structure is adopted. These two factors results in more severe hot carrier effects.

A lot of alternative approaches have to be used in order to tune threshold voltage. One of the alternatives is that the gate material should have a tunable work function. The metal gates with wide range of work functions have been used for threshold voltage adjustment of these devices. Further, metal gates offer many advantages over the poly-Si gates.

The GIDL current occurs in the deep depleted drain region underneath the gate region which is a major aspect of tunneling in MOSFETs. Behavior of GIDL current can be described by several mechanisms for example the indirect band-to-band tunneling model and the band-trap-band tunneling model. The band-to-band tunneling has been identified as the major leakage mechanism on the basis of qualitative agreements between experiments but in this section GIDL current is modeled analytically & simulations has been done. The GIDL current arises due to the potential difference applied between drain and gate. A strong depletion region is developed under the gate-to-drain overlap region. The presence of a gate-induced high electric field necessitates the overlap of silicon energy bands and causes the emission of minority carriers. These minority carriers will travel from the valence band to conduction band of silicon by band-to-band tunneling. The electrons emitted at the surface of the deep depletion layer are collected by the drain and move toward the substrate, under the transversal electric field effect. Band to Band tunneling is only possible in the presence of a high electric field in that region. The field in silicon at the Si–SiO_2 interface depends on the doping concentration in the diffusion region and the difference between V_D and V_G i.e. $V_{GD.}$ Band-to-band tunneling current density is the highest where the electric field is the largest. The theory of tunneling current predicts:

$$I_{gidl} = A.E_s \exp(-\frac{B}{E_s}) \quad (1)$$

where A is a constant and whose value is calculated as:

$$A = \frac{q^2 m_r^{1/2}}{18 .\pi .h^2 .E_{gap}^{3/2}} \quad (2)$$

and

$$B = \frac{\pi .m_r^{1/2} .E_{gap}^{3/2}}{2\sqrt{2}.q.\hbar} \quad (3)$$

where m_r=0.2m (electron effective mass) and E_{gap} is the direct energy band gap of silicon (3.5 ev).

By putting all the values in equation (3) value of B is calculated and we have B=21.3 MV/cm. E_s is the surface electric field at the tunneling point in the gate-to-drain overlap region and can be obtained as follows

$$E_s \approx \frac{V_{gd} - 1.2}{3T_{ox}} \quad (4)$$

This is the vertical electric field at silicon surface, "3" is the ratio of silicon permittivity to oxide permittivity, t_{ox} is the oxide thickness in the overlap region in centimeters and V_{GD} represents the gate to drain voltage in volts [3]. A bend bending of 1.2 eV is the minimum necessary for band-to-band tunneling to occur. With the help of equation (1), (2), (3) and (4) value of GIDL current is calculated as 1.24e-9 μA/m^2.

3. Analytical Model of GIDL

The work-function of gate material used for NMOS & PMOS devices is desirable for better conduction. In bulk CMOS, there exists possibility to engineer the work-function of metal gates to some extent around the poly-Si work-function. In this section, we present a mathematical analysis incorporating gate work-function in the equation for GIDL current. A simple analysis is presented to model the dependence of electric field in the gate-drain overlap region on the gate work-function [4]. This model represents description of GIDL & impact of work-function of poly-silicon gate on the performance of the device. The total electric field at any point in the drain depletion region is given by the vector sum of vertical and lateral fields.

$$E_{TOTAL}^2 = E_{VERT}^2 + E_{LAL}^2 \quad (5)$$

The vertical field (E_{ox}) across oxide or E_{si} across the Si-SiO_2 interface is given by [2] .

$$E_{ox} = \frac{(V_{DG} - V_{FB} - \psi_S)}{T_{ox}} \quad (6)$$

where V_{DG}= V_D-V_G i.e. the difference between drain and gate voltages, V_{FB}= (Φ_M- Φ_{si}) is the flat-band voltage, Φ_M is the gate work function, Φ_{si} is the silicon substrate work function, Tox is the thickness of gate oxide, and Ψ_S is the potential drop across the silicon for band-to-band tunneling and accounts for band-bending.

Using depletion approximation the vertical electric field E_{Si} can be expressed as

$$E_{si} = \frac{qN_D}{\varepsilon_{si}} \sqrt{\frac{2\varepsilon_{si}\psi_s}{qN_D}} \quad (7)$$

where N_D is impurity doping concentration in the drain region, ε_{si} is dielectric constant of the silicon, q is electron charge, and x is the coordinate normal to the Si-SiO2

interface. According to the Gaussian law, the electrical displacement across the Si-SiO2 interface must be continuous [5] . It can be expressed as

$$\varepsilon_{si}E_{si} = \varepsilon_{ox}E_{ox} = \varepsilon_{ox}\frac{(V_{DG} - V_{FB} - \psi_s)}{T_{ox}} \quad (8)$$

,

Combining equations (7) and (8) the band bending ψ_S can thus be calculated as:

$$\psi_s = V_{DG} - V_{FB} + \frac{qN_D T_{ox}^2 \varepsilon_{si}}{\varepsilon_{ox}^2}\sqrt{\left(\frac{qN_D T_{ox}^2 \varepsilon_{si}}{\varepsilon_{ox}^2} + (V_{DG} - V_{FB})\right)^2 - (V_{DG} - V_{FB})^2} \quad (9)$$

,

The lateral field (EY) can be expressed as

$$E_{Lat} = \frac{V_{DG}}{(\frac{\varepsilon_{si}}{\varepsilon_{ox}}T_{ox}h)^2} \quad (10)$$

,

where, ε_{ox} is the permittivity of oxide, h is the parameter related to junction depth as $h=10^{-4}r_j^{2/3}L^{2/5}/T_{ox}^{3/4}$ for Tox<150Ao, r_j is the junction depth, and L is the channel length. Using equations (6) and (10) in (5), we get

$$E_{Total}^2 = \frac{(V_{DG} - V_{FB} - \psi_s)^2}{T_{ox}^2} + \frac{V_{DG}^2}{\frac{\varepsilon_{si}}{\varepsilon_{ox}}T_{ox}h}$$

,

$$E_{Total}^2 = \frac{(V_{DG} - V_{FB} - \psi_s)^2}{T_{ox}^2} + \frac{V_{DG}^2}{\gamma T_{ox}h}$$

, where

$\gamma = \frac{\varepsilon_{si}}{\varepsilon_{ox}}$

,

$$E_{Total} = \sqrt{\frac{[\frac{V_{DG}}{T_{ox}}(1 - \frac{V_{FB} - \psi_s}{V_{DG}})^2 + \frac{V_{DG}^2}{\gamma h}]}{T_{ox}}} \quad (11)$$

Equation 11 gives the resultant electric field responsible for GIDL acting at any point in the gate-drain overlap region. The metal gate work-function can now be incorporated in the flat-band voltage and the equation 11 can be modified as

$$E_{Total} = \sqrt{\frac{[\frac{V_{DG}}{T_{ox}}(1 - \frac{[(\phi_M - \phi_{si}) + \psi_s]}{V_{DG}})^2 + \frac{V_{DG}^2}{\gamma h}]}{T_{ox}}}$$

The effect of gate work-function engineering on the resultant electric field in the gate-drain overlap region can be analyzed from equation (11) by substituting the work function of the metal being used as gate electrode as Φ_M in above equation [6]. It should be noted that Φ_{Si} in all the above equations refers to the Si drain work-function. According to the tunneling theory, the GIDL current can be expressed as

$$I_{GIDL} = AE_{GIDL}^2 \exp(\frac{-B}{E_{GIDL}}) \quad (12)$$

,

where E_{GIDL} is the field responsible for GIDL current, A a nd B are constants for indirect phonon assisted tunneling. S ubstituting the value for EGIDL from equation (13) in equ ation (14), we get

$$I_{GIDL} = A\sqrt{\frac{[\frac{V_{DG}}{T_{ox}}(1 - \frac{(\phi_M - \phi_{si}) - \psi_s}{V_{DG}})^2 + \frac{V_{DG}^2}{\gamma h}]}{T_{ox}}}\exp(\frac{-B}{\sqrt{\frac{[\frac{V_{DG}}{T_{ox}}(1 - \frac{(\phi_M - \phi_{si}) - \psi_s}{V_{DG}})^2 + \frac{V_{DG}^2}{\gamma h}]}{T_{ox}}}}) \quad (13)$$

.

The above equation 13 shows that GIDL current has both a quadratic and an exponential dependence on gate work-function of the device. The above equation can be applied to bulk as well as SOI CMOS alike. The modeled equation can hence be used to study the impact of using metal gate electrodes with wide range of work functions on the GIDL current as presented by the modeling predictions in the next section. Equation (14) is also the model for BTBT being currently used in the ATLAS device simulator [10]. Though it does not take into account the lateral electric field and the gate work-function, but is enough for evaluating dependence of GIDL on various parameters.

4. Design and Simulation of 90nm NMOS

The device used in this study was NMOS with n+ poly-Si fabricated by 90nm technology. The gate oxide thickness T_{ox} was 2nm. 90nm NMOS is simulated using process simulation in ATHENA having lightly doped substrate having concentration 1e15 (atoms/cm^3) and desired characteristics were extracted using ATLAS. Process simulation comprises the modeling of all process steps which are necessary for the fabrication of semiconductor devices. These process steps are layer deposition**,** lithography**,** etching**,** implantation**,** oxidation and diffusion [7]. The process simulation uses ATLAS as a simulator that provides general capabilities for numerical, physically-based, two-dimensional simulation of semiconductor processing [8].

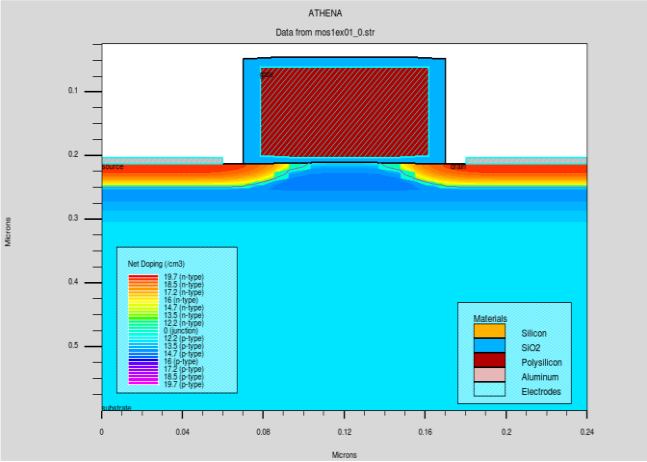

Figure 1. Structure of 90 nm MOSFET in Athena

Figure 1 shows the structure of 90nm NMOS with oxide thickness 2nm and effective channel length is measured as 55nm. The resulting physical structures are used as input by ATLAS, which then predicts the electrical characteristics associated with specified bias conditions. The combination of ATHENA and ATLAS simulator of SILVACO makes it feasible to extract the influence of process parameters on device characteristics.

5. Results and Discussions

This device is simulated on SILVACO-ATLAS and its characteristics has been analyzed and given below. Device simulation is applied to calculate the electrical behavior of semiconductor devices. The plot log Id–Vgs and Id-Vds characteristics at different drain voltages are given below in figures.

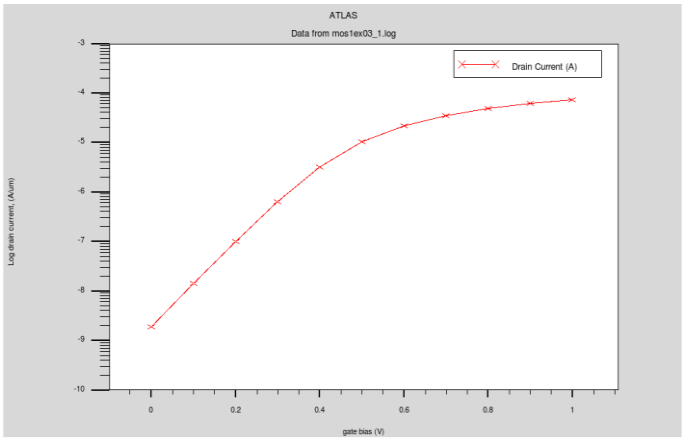

Figure 2 Log I_d-V_{gs} characteristics of 90nm MOSFET

Drain versus gate voltage (in log mode) characteristics of 90nm NMOS is shown in the above figure 2. It shows that as the gate voltage increases from 0 to 1 V drain current also increases linearly. Threshold voltage is measured as 0.36V in case of 90nm NMOS and graph for I_d-V_{gs} characteristics of 90nm NMOS is shown in the figure 3 below

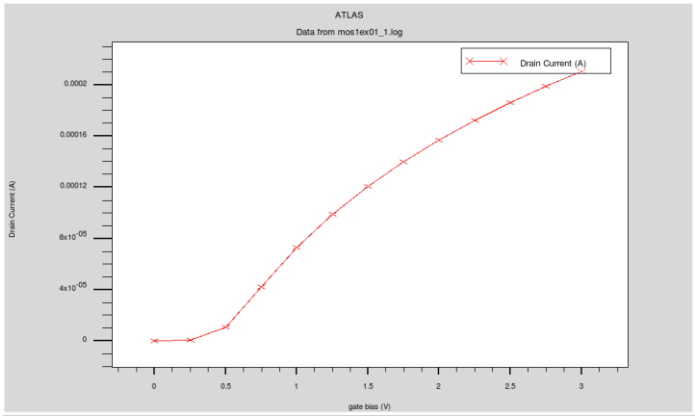

Figure 3 I_d – V_{gs} characteristic for 90nm n-channel NMOS

To extract the characteristic for drain current varying with gate voltage at fixed drain voltage we use ATLAS simulator and apply different drain voltages and vary gate voltage from -0.5 to 1V and then we get a graph log I_d versus Vg and then we estimate value of GIDL current from this graph and then compare this value with theoretical results.

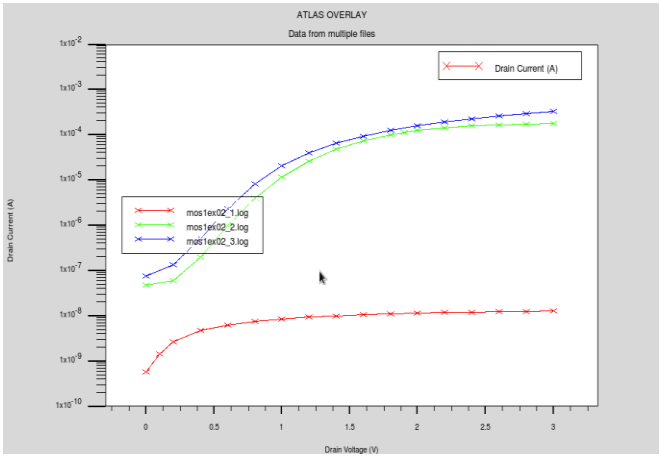

Figure 4 Log I_d-V_{ds}characteristics of 90nm MOSFET at different drain voltages

To reduce the leakage current in Nano-scale devices we have to reduce GIDL current also [13]. To reduce GIDL current LDD can be applied to the Nano-scale devices and also work-function engineering can be done. Work-function engineering is the method in which work-function of gate material in varied from 4.0 to 5.2 eV approximately and improvement in value of GIDL current is observed. Log Id-Vg characteristics of 90nm MOSFET (with LDD) at different drain voltages is shown in figure 5 below.

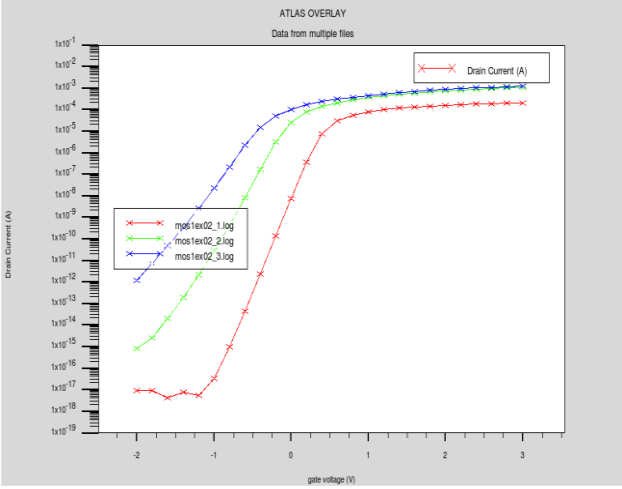

Figure 5 Log I_d-V_{gs} characteristics of 90nm MOSFET (with LDD) at different drain voltages

With the help of work-function engineering Log I_d-V_g characteristics at different work-function of gate material is shown in figure 6. This graph shows that as the work-function of gate material increases value of GIDL current decreases [9].

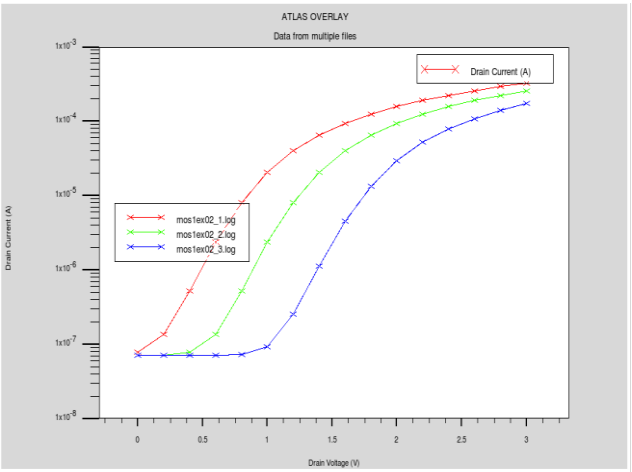

Figure 6 Log I_d-V_{ds} characteristics of 90nm MOSFET (with LDD) at different drain voltages with work-function engineering

6. Conclusion

The gate work-function is an important parameter to control the leakage current in field effect transistors. The work-function of NMOS device has been varied to control the GIDL current. The results also show that the gate work-function plays an important role to control of the GIDL current. The use of high-k gate dielectric with metal gates will have higher performance results as compared to using SiO2 gate dielectric as metals are generally more compatible with high-k gate dielectrics. The decrease in the resultant field and the GIDL current at high values of gate work-function suggests the use of gate work-function of 5.2 eV and higher if other methods of V_{th} control are used. Further, the results suggest that metal gate technology may become a performance booster for deep sub-micron low power operating devices.

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